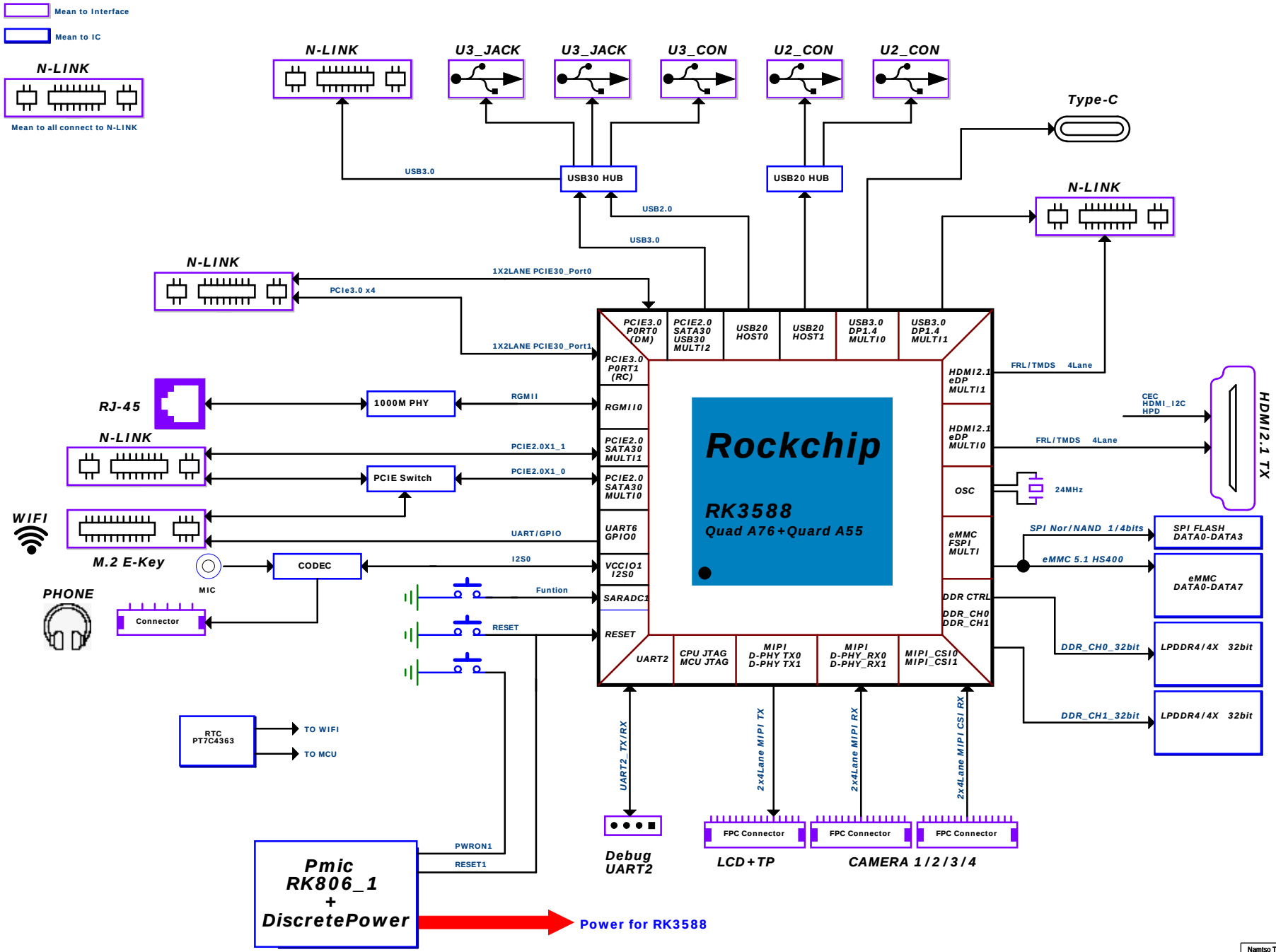
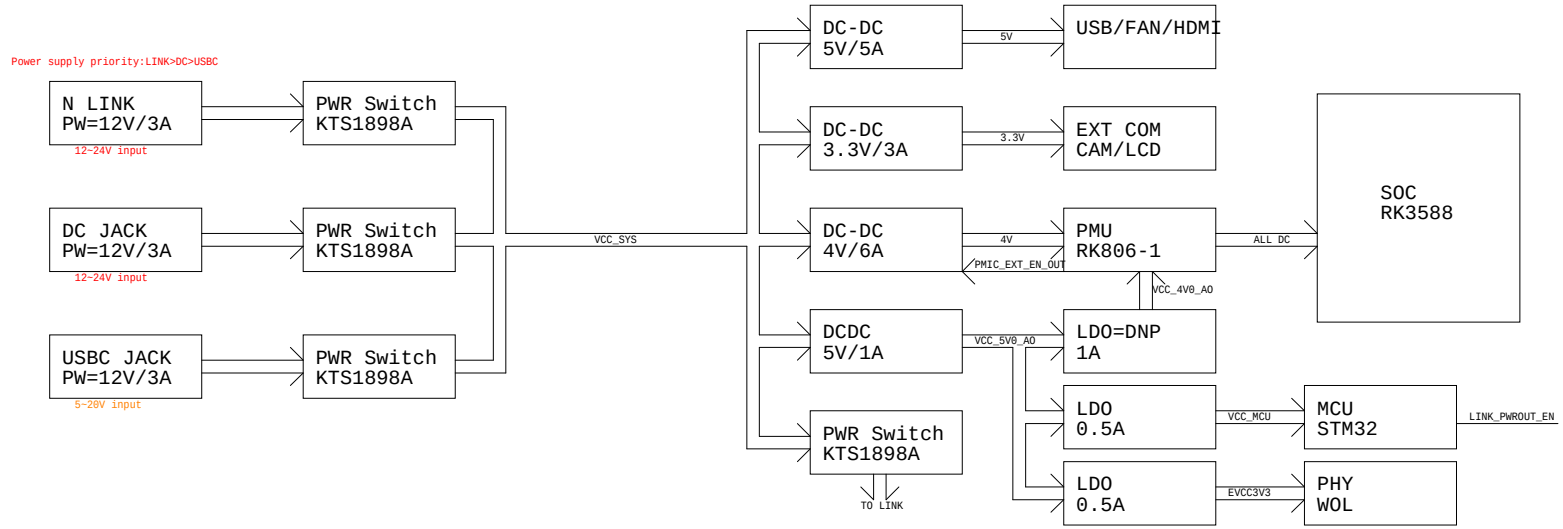
Namtso Technology Co., Ltd			
Project:	**A10**		
File:	Namtso LOGO		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	0



Namtso Technology Co., Ltd			
Project:	A10		
File:	Block		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Tonti Liang	Sheet:	1

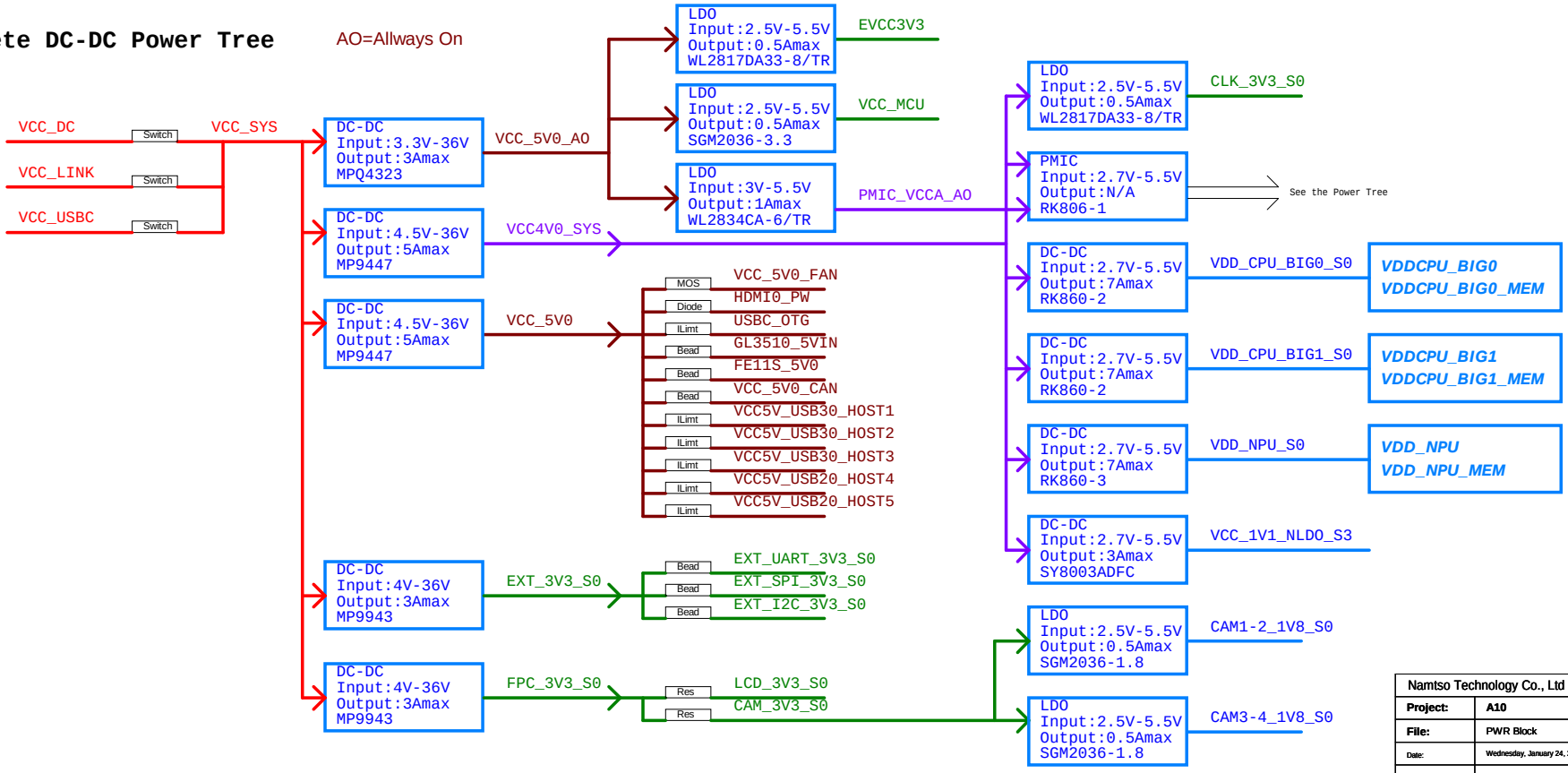
Power Block

DNP=Do Not Paste



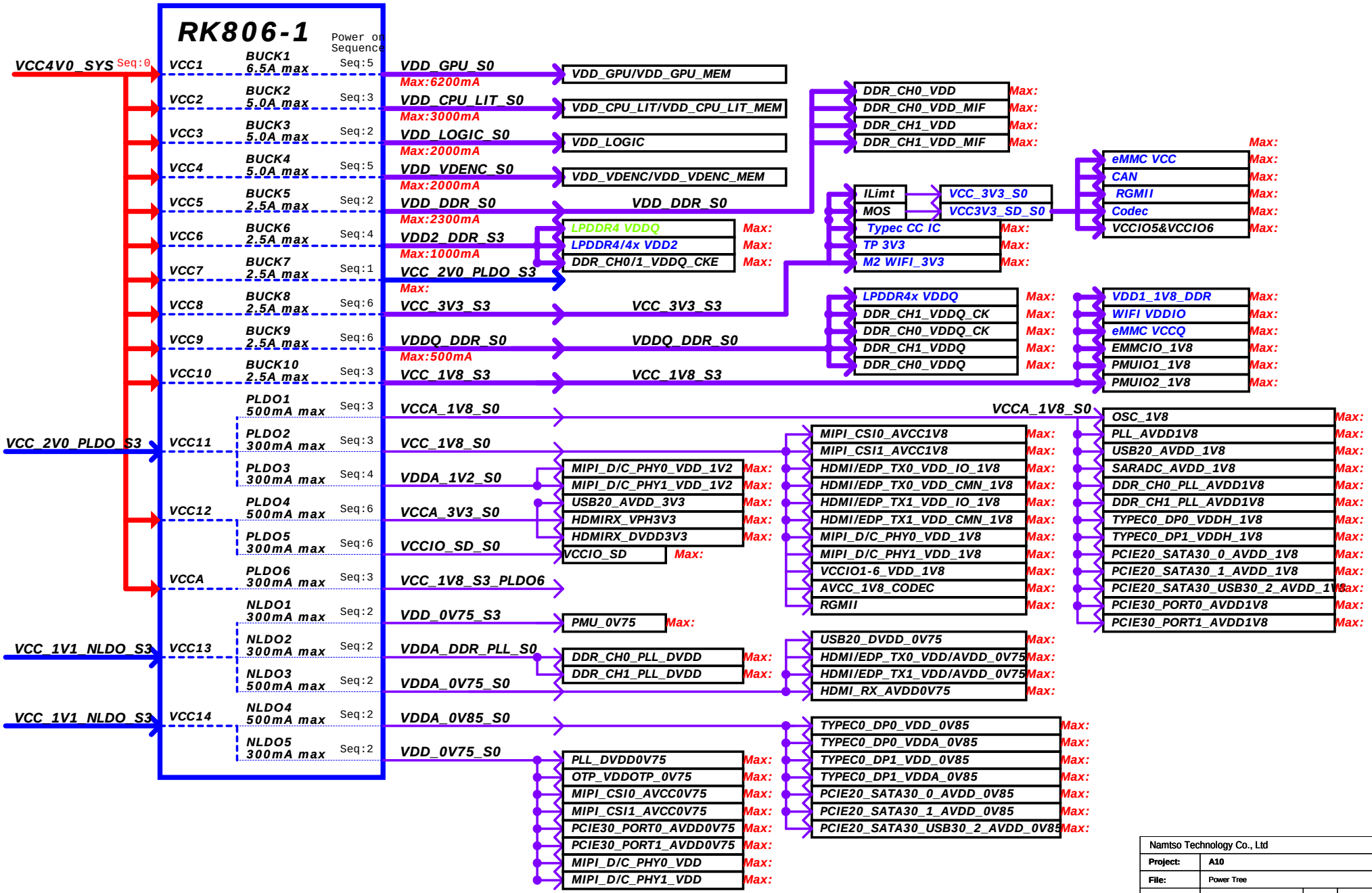
Discrete DC-DC Power Tree

AO=Allways On



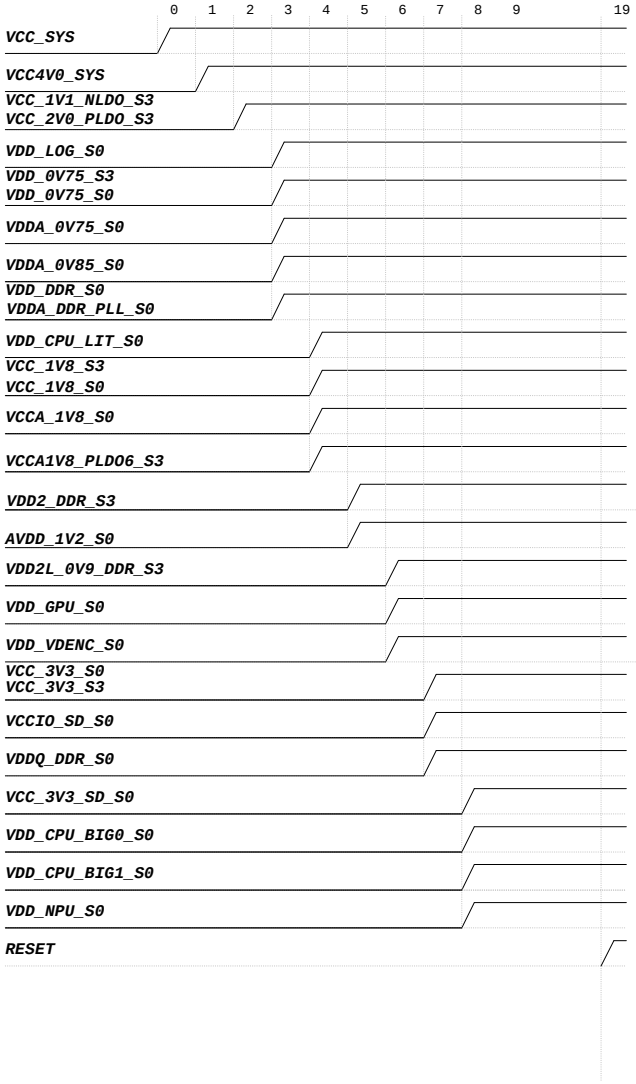
Namtso Technology Co., Ltd			
Project:	A10		
File:	PWR Block		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	2

PMIC Power Tree



Namtso Technology Co., Ltd			
Project:	A10		
File:	Power Tree		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	3

Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC4V0_SYS	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO	RK806-1_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD

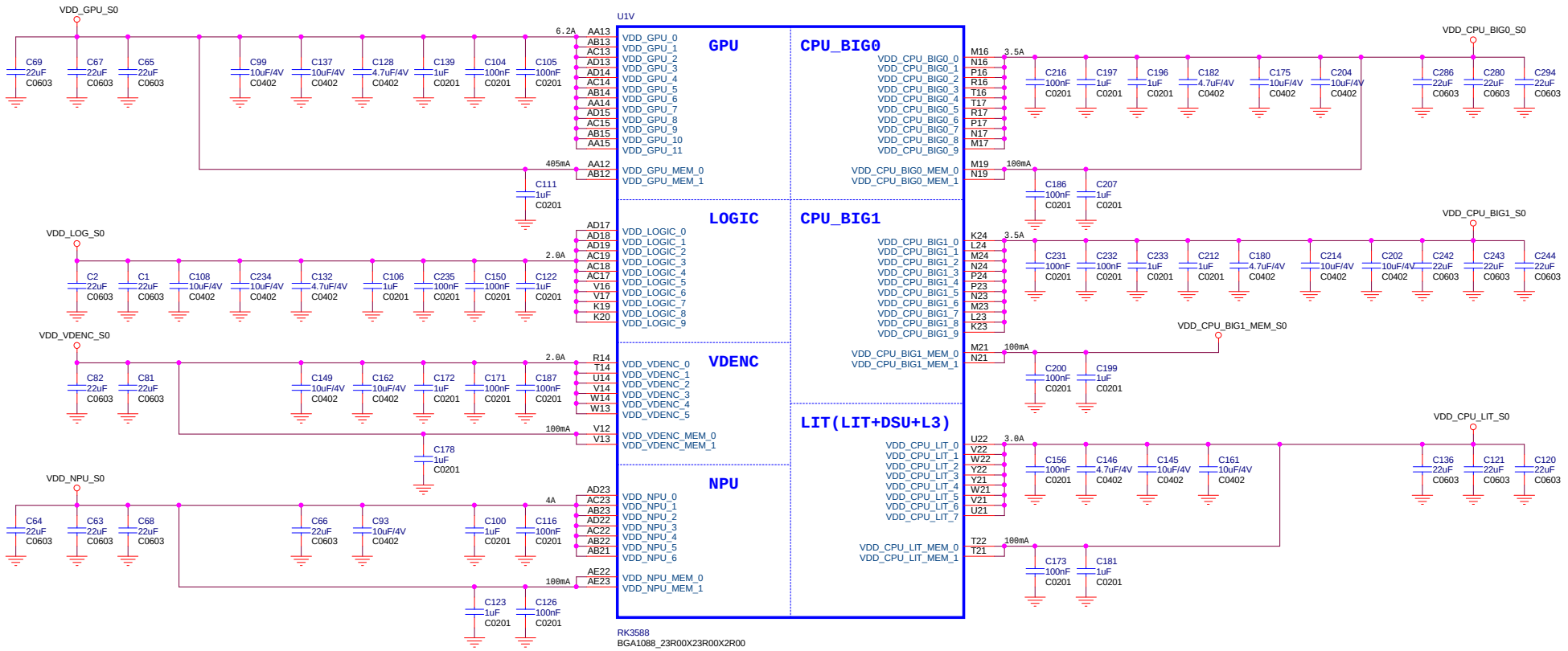
IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	IO Operating Voltage
PMUIO1	Pin N28	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin R27 Pin P28	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8_S3	1.8V
EMMCIO	Pin V26	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin G20	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AA7 Pin Y7	1.8V or 3.3V	VCCIO2_1V8 VCCIO2	VCC_1V8_S0 VCC_IO_SD	1.8V/3.3V
VCCIO3	Pin Y26	1.8V Only	VCCIO3_1V8	VCC_1V8_S3	1.8V
VCCIO4	Pin H20 Pin H21	1.8V or 3.3V	VCCIO4_1V8 VCCIO4	VCC_1V8_S0 VCC_1V8_S0	1.8V
VCCIO5	Pin W25 Pin W26	1.8V or 3.3V	VCCIO5_1V8 VCCIO5	VCC_1V8_S0 VCC_3V3_S0	3.3V
VCCIO6	Pin AC25 Pin AC26	1.8V or 3.3V	VCCIO6_1V8 VCCIO6	VCC_1V8_S0 VCC_3V3_S0	3.3V

IO Type	Operating Voltage
1.8V Only	VCCIO*_1V8=1.8V
1.8V or 3.3V	VCCIO*_1V8=1.8V VCCIO*=1.8V or 3.3V

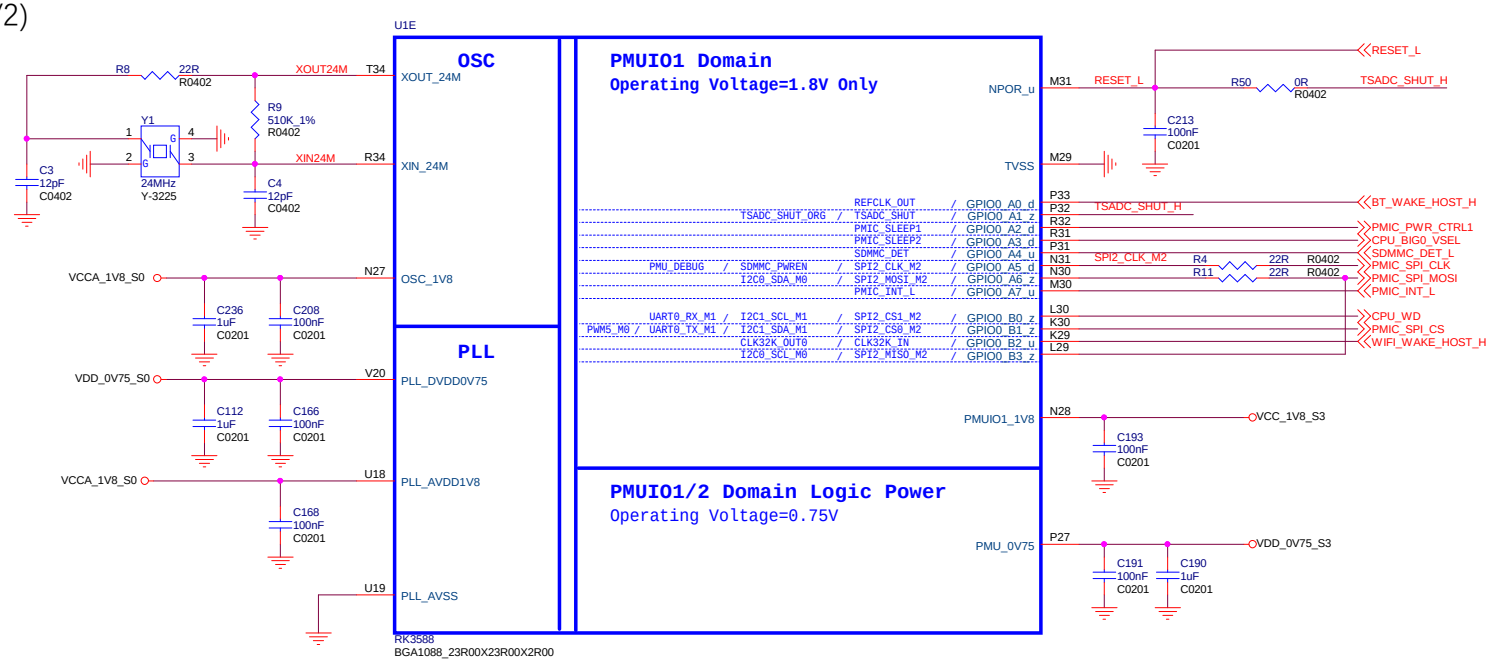
Namtso Technology Co., Ltd			
Project:	A10		
File:	Power Sequence		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	4

RK3588_V(POWER)

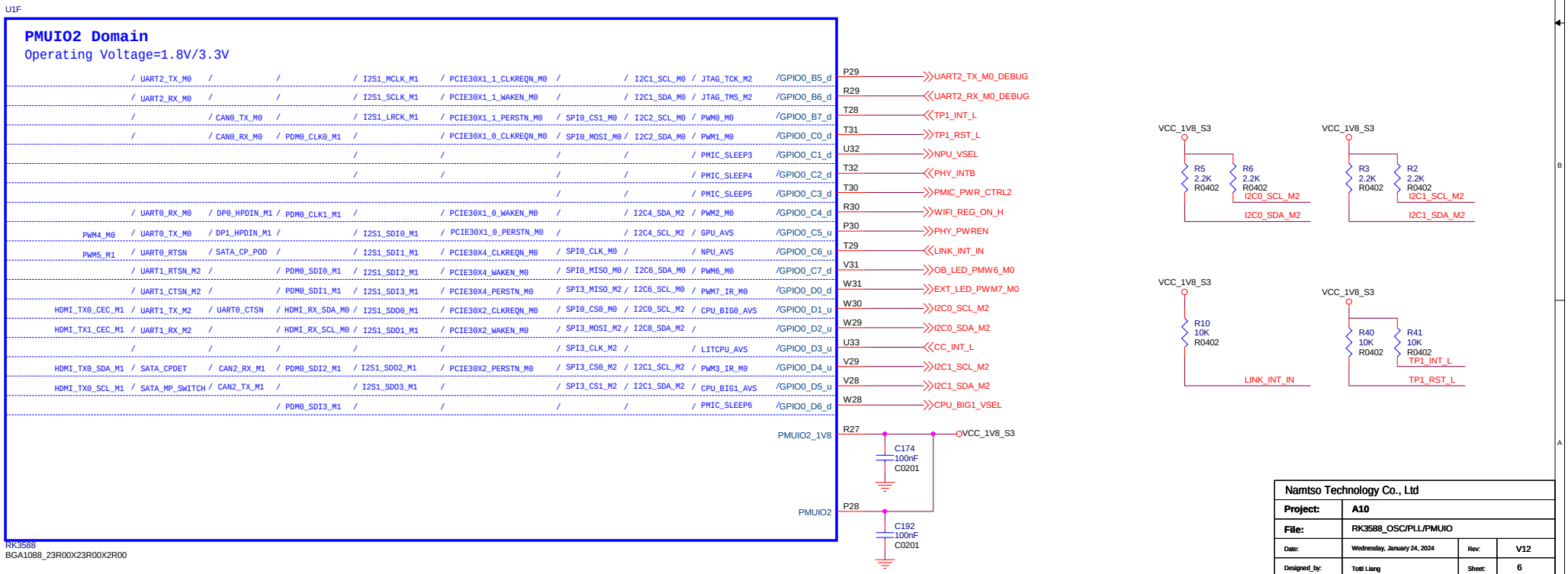


Namtso Technology Co., Ltd			
Project:	A10		
File:	RK3588_Power		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	5

RK3588_E(OSC/PLL/PMUIO1/2)



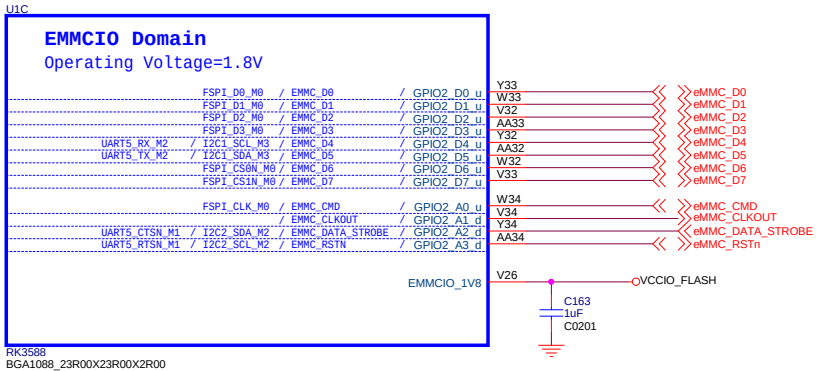
RK3588_F(PMUIO2)



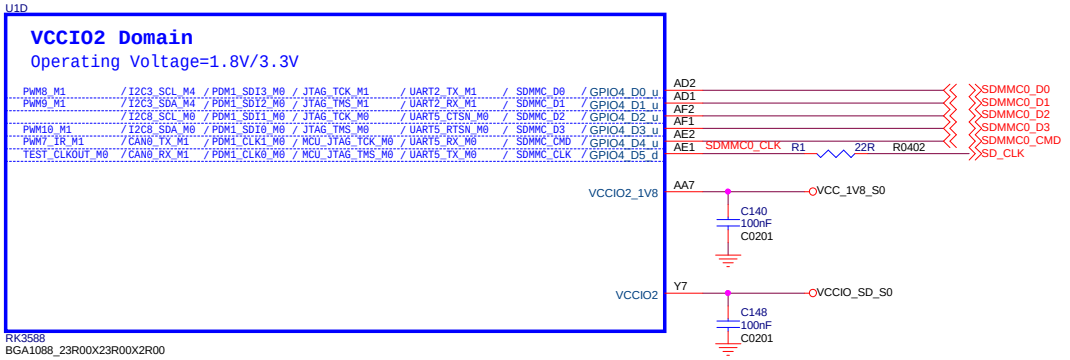
Namtso Technology Co., Ltd			
Project:	A10		
File:	RK3588_OSC/PLL/PMUIO		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	6

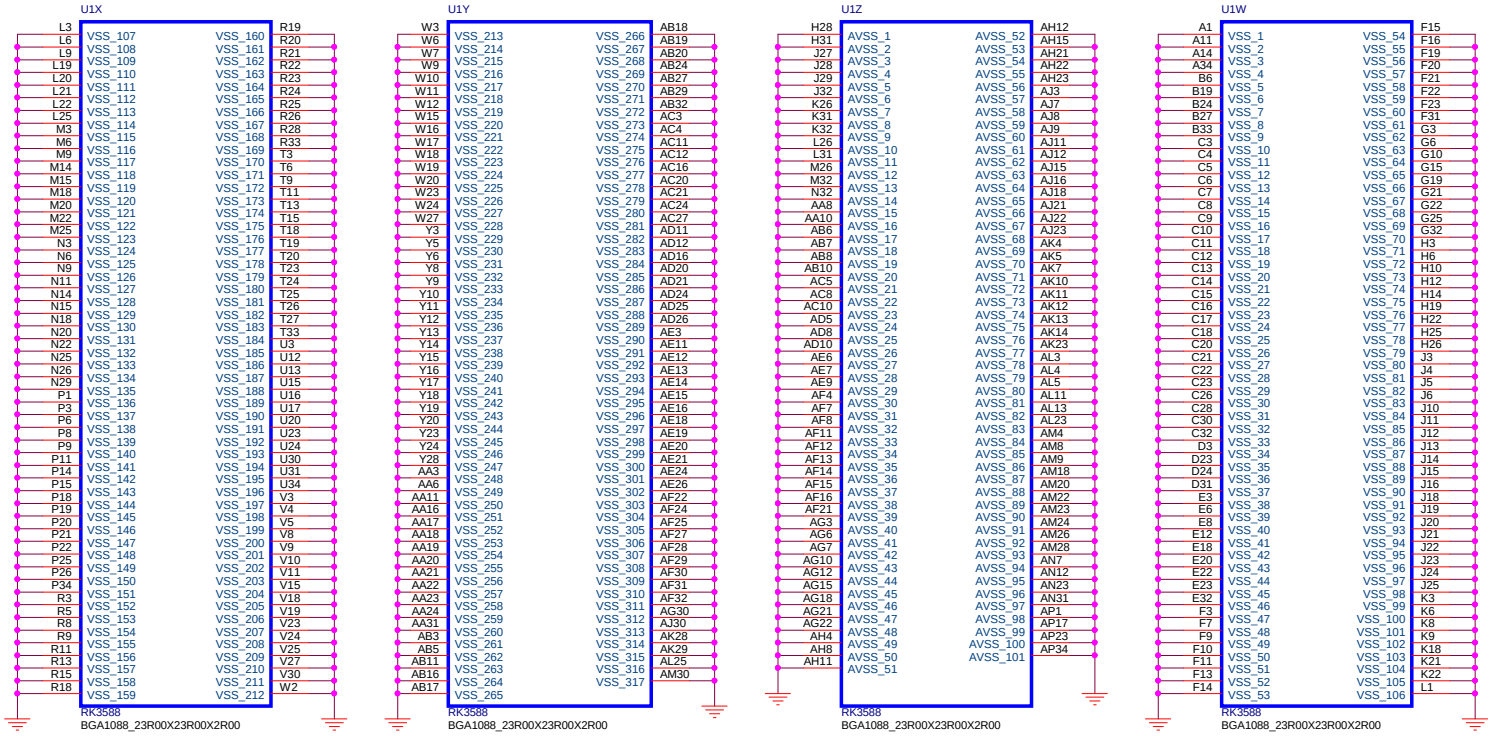

U1A
DDR_CH0_DQ0_A
DDR_CH0_DQ1_A
DDR_CH0_DQ2_A
DDR_CH0_DQ3_A
DDR_CH0_DQ4_A
DDR_CH0_DQ5_A
DDR_CH0_DQ6_A
DDR_CH0_DQ7_A
DDR_CH0_DQ8_A
DDR_CH0_DQ9_A
DDR_CH0_DQ10_A
DDR_CH0_DQ11_A
DDR_CH0_DQ12_A
DDR_CH0_DQ13_A
DDR_CH0_DQ14_A
DDR_CH0_DQ15_A
DDR_CH0_DM0_A
DDR_CH0_DM1_A
DDR_CH0_DQS0P_A
DDR_CH0_DQS0N_A
DDR_CH0_DQS1P_A
DDR_CH0_DQS1N_A
DDR_CH0_WCK0P_A
DDR_CH0_WCK0N_A
DDR_CH0_WCK1P_A
DDR_CH0_WCK1N_A
DDR_CH0_A0_A
DDR_CH0_A1_A
DDR_CH0_A2_A
DDR_CH0_A3_A
DDR_CH0_A4_A
DDR_CH0_A5_A
DDR_CH0_A6_A
DDR_CH0_CLKP_A
DDR_CH0_CLKN_A
DDR_CH0_LP4/4X_CKE0/LP5_CS0_A
DDR_CH0_LP4/4X_CKE1/LP5_CS1_A
DDR_CH0_LP4/4X_CS0_A
DDR_CH0_LP4/4X_CS1_A
DDR_RESET
VDDQ_DDR_S0
R42
240R_1%
R0201
DDR_CH0_CK_A
DDR_CH0_CKB_A
DDR_CH0_ZQ_A
DDR_CH0_RESET_A
DDR_CH0_DQ0_B
DDR_CH0_DQ1_B
DDR_CH0_DQ2_B
DDR_CH0_DQ3_B
DDR_CH0_DQ4_B
DDR_CH0_DQ5_B
DDR_CH0_DQ6_B
DDR_CH0_DQ7_B
DDR_CH0_DQ8_B
DDR_CH0_DQ9_B
DDR_CH0_DQ10_B
DDR_CH0_DQ11_B
DDR_CH0_DQ12_B
DDR_CH0_DQ13_B
DDR_CH0_DQ14_B
DDR_CH0_DQ15_B
DDR_CH0_DM0_B
DDR_CH0_DM1_B
DDR_CH0_DQS0P_B
DDR_CH0_DQS0N_B
DDR_CH0_DQS1P_B
DDR_CH0_DQS1N_B
DDR_CH0_WCK0P_B
DDR_CH0_WCK0N_B
DDR_CH0_WCK1P_B
DDR_CH0_WCK1N_B
DDR_CH0_A0_B
DDR_CH0_A1_B
DDR_CH0_A2_B
DDR_CH0_A3_B
DDR_CH0_A4_B
DDR_CH0_A5_B
DDR_CH0_CLKP_B
DDR_CH0_CLKN_B
DDR_CH0_LP4/4X_CKE0/LP5_CS0_B
DDR_CH0_LP4/4X_CKE1/LP5_CS1_B
DDR_CH0_LP4/4X_CS0_B
DDR_CH0_LP4/4X_CS1_B
R52
240R_1%
R0201
VDDQ_DDR_S0
DDR_PLL POWER
DDR_CH0_PLL_DVDD
0.75V-0.85V
DDR_CH0_PLL_AVDD1V8
1.8V
DDR_CH0_PLL_AVSS
VDDA_DDR_PLL_S0
VCCA_1V8_S0
LP4/4X_CKE&LP5_CS & Reset Power
LPDDR4/4X=1.1V
LPDDR5=1.05V
DDR_CH0_VDDQ_CKE
VDDQ_DDR_CKE_S3
MEMORY INTERFACE POWER
DDR_CH0_VDD_MIF_0
DDR_CH0_VDD_MIF_1
0.75V-0.85V
VDD_DDR_S0
CK Power
LPDDR4/4X=0.6V
LPDDR5=0.5V
DDR_CH0_VDDQ_CK
VDDQ_DDR_CK_S0
DIGITAL CORE POWER
DDR_CH0_VDD_0
DDR_CH0_VDD_1
DDR_CH0_VDD_2
DDR_CH0_VDD_3
0.75V-0.85V
DDR IO POWER
(Except for ck, cke and reset)
LPDDR4/4X=0.6V
LPDDR5=0.5V
DDR_CH0_VDDQ_0
DDR_CH0_VDDQ_1
DDR_CH0_VDDQ_2
DDR_CH0_VDDQ_3
DDR_CH0_VDDQ_4
VDDQ_DDR_S0
RK3588
BGA1088_23R00X23R00X2R00
U1B
DDR_CH1_DQ0_C
DDR_CH1_DQ1_C
DDR_CH1_DQ2_C
DDR_CH1_DQ3_C
DDR_CH1_DQ4_C
DDR_CH1_DQ5_C
DDR_CH1_DQ6_C
DDR_CH1_DQ7_C
DDR_CH1_DQ8_C
DDR_CH1_DQ9_C
DDR_CH1_DQ10_C
DDR_CH1_DQ11_C
DDR_CH1_DQ12_C
DDR_CH1_DQ13_C
DDR_CH1_DQ14_C
DDR_CH1_DQ15_C
DDR_CH1_DM0_C
DDR_CH1_DM1_C
DDR_CH1_DQS0P_C
DDR_CH1_DQS0N_C
DDR_CH1_DQS1P_C
DDR_CH1_DQS1N_C
DDR_CH1_WCK0P_C
DDR_CH1_WCK0N_C
DDR_CH1_WCK1P_C
DDR_CH1_WCK1N_C
DDR_CH1_A0_C
DDR_CH1_A1_C
DDR_CH1_A2_C
DDR_CH1_A3_C
DDR_CH1_A4_C
DDR_CH1_A5_C
DDR_CH1_CLKP_C
DDR_CH1_CLKN_C
DDR_CH1_LP4/4X_CKE0/LP5_CS0_C
DDR_CH1_LP4/4X_CKE1/LP5_CS1_C
DDR_CH1_LP4/4X_CS0_C
DDR_CH1_LP4/4X_CS1_C
VDDQ_DDR_S0
R53
240R_1%
R0201
DDR_CH1_CK_C
DDR_CH1_CKB_C
DDR_CH1_ZQ_C
DDR_CH1_RESET_C
DDR_CH1_DQ0_D
DDR_CH1_DQ1_D
DDR_CH1_DQ2_D
DDR_CH1_DQ3_D
DDR_CH1_DQ4_D
DDR_CH1_DQ5_D
DDR_CH1_DQ6_D
DDR_CH1_DQ7_D
DDR_CH1_DQ8_D
DDR_CH1_DQ9_D
DDR_CH1_DQ10_D
DDR_CH1_DQ11_D
DDR_CH1_DQ12_D
DDR_CH1_DQ13_D
DDR_CH1_DQ14_D
DDR_CH1_DQ15_D
DDR_CH1_DM0_D
DDR_CH1_DM1_D
DDR_CH1_DQS0P_D
DDR_CH1_DQS0N_D
DDR_CH1_DQS1P_D
DDR_CH1_DQS1N_D
DDR_CH1_WCK0P_D
DDR_CH1_WCK0N_D
DDR_CH1_WCK1P_D
DDR_CH1_WCK1N_D
DDR_CH1_A0_D
DDR_CH1_A1_D
DDR_CH1_A2_D
DDR_CH1_A3_D
DDR_CH1_A4_D
DDR_CH1_A5_D
DDR_CH1_CLKP_D
DDR_CH1_CLKN_D
DDR_CH1_LP4/4X_CKE0/LP5_CS0_D
DDR_CH1_LP4/4X_CKE1/LP5_CS1_D
DDR_CH1_LP4/4X_CS0_D
DDR_CH1_LP4/4X_CS1_D
R54
240R_1%
R0201
VDDQ_DDR_S0
DDR_PLL POWER
DDR_CH1_PLL_DVDD
0.75V-0.85V
DDR_CH1_PLL_AVDD1V8
1.8V
DDR_CH1_PLL_AVSS
VDDA_DDR_PLL_S0
VCCA_1V8_S0
LP4/4X_CKE&LP5_CS & Reset Power
LPDDR4/4X=1.1V
LPDDR5=1.05V
DDR_CH1_VDDQ_CKE
VDDQ_DDR_CKE_S3
MEMORY INTERFACE POWER
DDR_CH1_VDD_MIF_0
DDR_CH1_VDD_MIF_1
0.75V-0.85V
VDD_DDR_S0
CK Power
LPDDR4/4X=0.6V
LPDDR5=0.5V
DDR_CH1_VDDQ_CK
VDDQ_DDR_CK_S0
DIGITAL CORE POWER
DDR_CH1_VDD_0
DDR_CH1_VDD_1
DDR_CH1_VDD_2
DDR_CH1_VDD_3
0.75V-0.85V
DDR IO POWER
(Except for ck, cke and reset)
LPDDR4/4X=0.6V
LPDDR5=0.5V
DDR_CH1_VDDQ_0
DDR_CH1_VDDQ_1
DDR_CH1_VDDQ_2
DDR_CH1_VDDQ_3
DDR_CH1_VDDQ_4
VDDQ_DDR_S0
RK3588
BGA1088_23R00X23R00X2R00
DDR FILTER
VDDQ_DDR_S0
VDDQ_DDR_CK_S0
C169 10uF/4V C0402
C246 1uF C0201
C184 1uF C0201
C245 100nF C0201
C249 100nF C0201
C248 100nF C0201
C221 1uF C0201
VCCA_1V8_S0
VDDA_DDR_PLL_S0
VDDQ_DDR_CKE_S3
C206 1uF C0201
C201 1uF C0201
C211 1uF C0201
VDD_DDR_S0
C158 10uF/4V C0402
C159 4.7uF/4V C0402
C177 100nF C0201
VDD_DDR_S0
C215 1uF C0201
C195 100nF C0201
VDDQ_DDR_S0
VDDQ_DDR_CK_S0
C239 10uF/4V C0402
C247 1uF C0201
C176 1uF C0201
C205 100nF C0201
C194 100nF C0201
C217 100nF C0201
C209 1uF C0201
C275 10uF C0402
VCCA_1V8_S0
VDDA_DDR_PLL_S0
VDDQ_DDR_CKE_S3
C230 1uF C0201
C219 1uF C0201
C256 1uF C0201
VDD_DDR_S0
C222 10uF/4V C0402
C220 4.7uF/4V C0402
C225 100nF C0201
VDD_DDR_S0
C198 1uF C0201
C185 100nF C0201
Namtso Technology Co., Ltd
Project: A10
File: RK3588_DDR Controler
Date: Wednesday, January 24, 2024
Rev: V12
Designed_by: Totti Liang
Sheet: 7

RK3588_C(EMMCIO Domain)



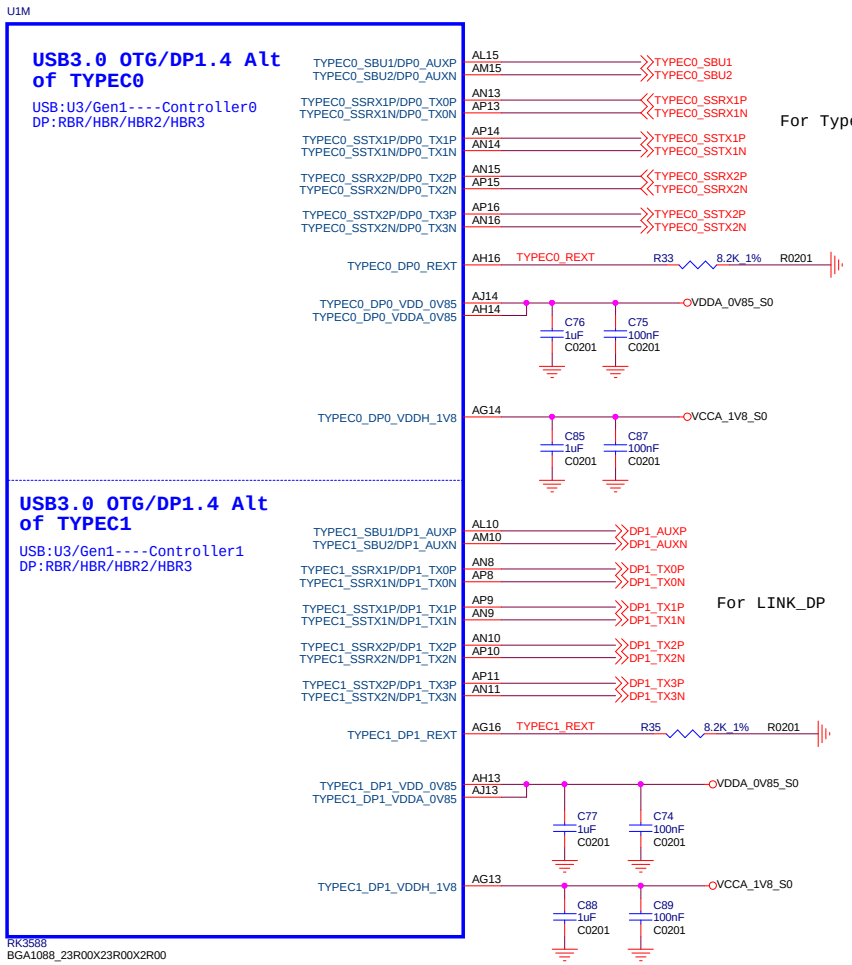
RK3588_D(VCCIO2 Domain)





Namtso Technology Co., Ltd			
Project:	A10		
File:	RK3588_Flash/GND		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	8

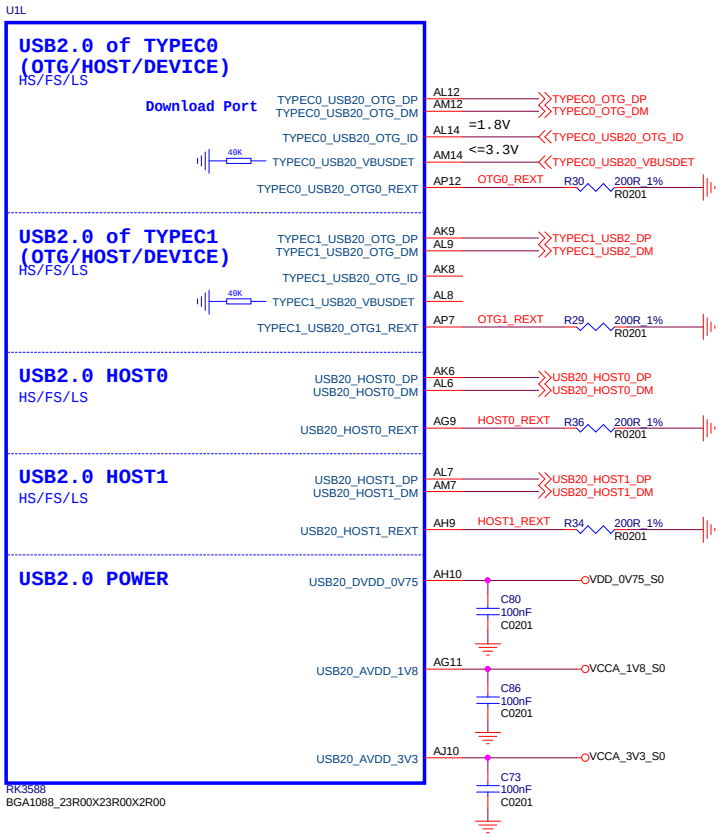
RK3588_M(TYPEC/DP)



USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*USB30 x4Lane*	*TYPEC_SSTX1P/1N&TYPEC_SSRX1P/1N or TYPEC_SSTX2P/2N&TYPEC_SSRX2P/2N*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:Lane0 Lane1 DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:Lane2 Lane3 DP:Lane0 Lane1*

RK3588_L(USB2.0 HOST/OTG)



Note:

TYPEC0_USB20_OTG:

DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

TYPEC1_USB20_OTG:

If not used:
DP/DM:Leave floating
ID:Leave floating
VBUSDET:Leave floating
REXT:Leave floating
Power:Leave floating

USB20_HOST0/USB20_HOST1:

If not used:
DP/DM:Leave floating
REXT:Leave floating
Power:Leave floating

Namtso Technology Co., Ltd			
Project:	**A10**		
File:	**RK3588_USB30/USB20**		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	9

RK3588_G(VCCIO1 Domain)

U1G

VCCIO1 Domain
Operating Voltage=1.8V

SPI4_MISO_M0	UART3_RX_M0		I2C3_SDA_M0		GPIO1_C0_z
SPI4_MOSI_M0	UART3_TX_M0		I2C3_SCL_M0		GPIO1_C1_z
SPI4_CLK_M0	UART3_RTSN	PWM3_IR_M2	I2C6_SDA_M1	I2S0_MCLK	GPIO1_C2_d
SPI4_CS0_M0	UART3_CTSN	PWM7_IR_M2	I2C6_SCL_M1	I2S0_SCLK	GPIO1_C3_d
SPI4_CS1_M0		PWM11_IR_M2	I2C2_SDA_M3	PDM0_CLK1_M0	GPIO1_C4_d
	UART4_RTSN		I2C2_SCL_M3	I2S0_LRCK	GPIO1_C5_d
		PWM15_IR_M2	I2C4_SDA_M4	PDM0_CLK0_M0	GPIO1_C6_d
	UART4_CTSN		I2C4_SCL_M4	I2S0_SDO0	GPIO1_C7_d
SPI1_MISO_M2	UART6_TX_M2		I2C7_SCL_M0	I2S0_SDO1	GPIO1_D0_d
SPI1_MOSI_M2	UART6_RX_M2		I2C7_SDA_M0	PDM0_SDI1_M0	I2S0_SDO2/I2S0_SDI3 GPIO1_D1_d
SPI1_CLK_M2	UART4_TX_M0	PWM0_M1	I2C1_SCL_M4	PDM0_SDI2_M0	I2S0_SDO3/I2S0_SDI2 GPIO1_D2_d
SPI1_CS0_M2	UART4_RX_M0	PWM1_M1	I2C1_SDA_M4	PDM0_SDI3_M0	I2S0_SDI1 GPIO1_D3_d
					I2S0_SDI0 GPIO1_D4_d
SPI1_CS1_M2				PDM0_SDI0_M0	GPIO1_D5_d

VCCIO1_1V8

G29 I2C3_SDA_M0
G27 I2C3_SCL_M0
F30 I2S0_MCLK
E31 I2S0_SCLK
E30 HP_DET_L
D30 I2S0_LRCK
D29 CAM4_PDN
E29 I2S0_SDO0
F26 SPI1_MISO_M2
F27 SPI1_MOSI_M2
F28 SPI1_CLK_M2
E28 SPI1_CS0_M2
D28 I2S0_SDI0
G26 GSENSOR_INT_L

G20 — VCC_1V8_S0

C257 100nF C0201

RK3588
BGA1088_23R00X23R00X2R00

VCC_1V8_S0
R16 2.2K R0402
R17 2.2K R0402
I2C3_SCL_M0
I2C3_SDA_M0

RK3588_H(VCCIO3 Domain)

U1H

VCCIO3 Domain
Operating Voltage=1.8V

	UART6_RX_M0	FSPI_D0_M1	SDIO_D0_M0	GMAC0_RXD2	GPIO2_A6_u
	UART6_TX_M0	FSPI_D1_M1	SDIO_D1_M0	GMAC0_RXD3	GPIO2_A7_u
I2C8_SCL_M1	UART6_RTSN_M0	FSPI_D2_M1	SDIO_D2_M0	GMAC0_RXCLK	GPIO2_B0_u
I2C8_SDA_M1	UART6_CTSN_M0	FSPI_D3_M1	SDIO_D3_M0	GMAC0_TXD2	GPIO2_B1_u
I2C3_SCL_M3			SDIO_CMD_M0	GMAC0_TXD3	GPIO2_B2_u
I2C3_SDA_M3		FSPI_CLK_M1	SDIO_CLK_M0	GMAC0_TXCLK	GPIO2_B3_d
I2C4_SDA_M1	UART7_RX_M0	FSPI_CS0N_M1	HDMI_TX1_SDA_M0	GMAC0_PTP_REFCLK	GPIO2_B4_u
I2C4_SCL_M1	UART7_TX_M0	FSPI_CS1N_M1	HDMI_TX1_SCL_M0	GMAC0_PPSTRIG	GPIO2_B5_u
I2C5_SCL_M4	UART1_RX_M0		I2S2_MCLK_M0	GMAC0_TXD0	GPIO2_B6_d
I2C5_SDA_M4	UART1_TX_M0		I2S2_SCLK_M0	GMAC0_TXD1	GPIO2_B7_d
I2C2_SDA_M1	UART1_RTSN_M0	SPI1_CLK_M0	I2S2_LRCK_M0	GMAC0_TXEN	GPIO2_C0_d
I2C2_SCL_M1	UART1_CTSN_M0	SPI1_MISO_M0		GMAC0_RXD0	GPIO2_C1_d
I2C6_SDA_M2	UART9_TX_M0	SPI1_MOSI_M0		GMAC0_RXD1	GPIO2_C2_d
I2C6_SCL_M2		SPI1_CS0_M0	I2S2_SDI_M0	ETH0_REFCLKO_25M	GPIO2_C3_d
TEST_CLKOUT_M1	UART9_RX_M0	SPI1_CS1_M0	HDMI_TX1_CEC_M0	GMAC0_PPSCLK	GPIO2_C4_d
				CLK32K_OUT1	GPIO2_C5_d
	UART7_RTSN_M0	SPI3_CS0_M0	PWM2_M2	GMAC0_RXDV_CRS	GPIO4_C2_d
I2C7_SCL_M1	PWM4_M1	SPI3_CS1_M0	I2S2_SDO_M0	GMAC0_MCLKINOUT	GPIO4_C3_d
I2C7_SDA_M1	UART9_RTSN_M0	SPI3_MISO_M0	PWM5_M2	GMAC0_MDC	GPIO4_C4_d
I2C8_SCL_M1	UART9_CTSN_M0	SPI3_MOSI_M0	PWM6_M2	GMAC0_MDIO	GPIO4_C5_d
I2C8_SDA_M1	UART7_CTSN_M0	SPI3_CLK_M0	PWM7_IR_M3	GMAC0_TXER	GPIO4_C6_d

VCCIO3_1V8

AC32 GPIO2_A6_u
AC31 GPIO2_A7_u
AE32 GPIO2_B0_u
AC33 GPIO2_B1_u
AC34 USB_HOST_PWREN_H
AE33 GPIO2_B3_d
AB31 GPIO2_B4_u
AB30 LINK/M2-PCIE_SW
AD33 TYPEC0_PWR_EN
AD34 EXT_3V3_EN
AE34 TP2_INT_L
AD32 TP2_RST_L
AD31 I2C6_SDA_M2
AD30 I2C6_SCL_M2
AC30
AE30 PCIE_PWREN_H
AE31 SPI3_CS0_M0
AF34 EXT_PWM4_M1
AB34 SPI3_MISO_M0
AB33 SPI3_MOSI_M0
AF33 SPI3_CLK_M0

Y26 — R7 0R R0402 — VCC_1V8_S3

C167 100nF C0201

RK3588
BGA1088_23R00X23R00X2R00

IO PIN	BT Used	FSPI Used
MCU_SPI/BT_SW		
CPU_SPI/BT_SW	L	H
GPIO2_A6_u	UART6_RX_M0_BT	FSPI_D0_M1
GPIO2_A7_u	UART6_TX_M0_BT	FSPI_D1_M1
GPIO2_B0_u	UART6_RTSn_M0_BT	FSPI_D2_M1
GPIO2_B1_u	UART6_CTSn_M0_BT	FSPI_D3_M1
GPIO2_B3_d	HOST_WAKE_BT_H	FSPI_CLK_M1
GPIO2_B4_u	BT_REG_ON_H	FSPI_CS0N_M1

VCC_1V8_S3
R43 10K R0402
R44 10K R0402
TP2_INT_L
TP2_RST_L

VCC_1V8_S3
R22 2.2K R0402
R25 2.2K R0402
I2C6_SCL_M2
I2C6_SDA_M2

RK3588_U(SARADC/OTP)

U1U

SARADC
12-bit 1MS/s

SARADC_IN0_BOOT Recovery/ SARADC_IN1
SARADC_IN2
SARADC_IN3
SARADC_IN4
SARADC_IN5
SARADC_IN6
SARADC_IN7
SARADC_AVDD_1V8

AM16 BOOT_SARADC_IN0
AL16 KEY_SARADC_IN1
AK16
AN17 EXT_SARADC_IN3
AM17
AK15 SARADC_IN5_HW_ID
AL17
AK17
AH18 — VCCA_1V8_S0

R26 10K R0402 — VCCA_1V8_S0
C61 1nF C0402
C62 1nF C0402
C70 1nF C0402
C60 1nF C0402

BOOT_SARADC_IN0
KEY_SARADC_IN1
EXT_SARADC_IN3

C91 100nF C0201

OTP

NC AD4 — Must floating

OTP_VDDOTP_0V75 AD3 — VDD_0V75_S0

C113 100nF C0201

TSADC

TSADC_TEST_OUT_TS AF18

RK3588
BGA1088_23R00X23R00X2R00

BOOT MODE CONFIG

VCCA_1V8_S0
R27 100K_1% R0402
BOOT_SARADC_IN0
R28 100K_1% R0402 DNP

TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	DNP	100K	0	0V	USB (Maskrom mode)
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	100K	51K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	100K	200K	2730	1.2V	FSPI M1-USB
LEVEL6	100K	499K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

BOARD ID CONFIG

VCCA_1V8_S0
R20 100K_1% R0402
SARADC_IN5_HW_ID
R21 51K_1% R0402

TABLE 2

Item	Rup	Rdown	ADC	VOL	VERSION
LEVEL1	DNP	100K	0	0V	V1.0
LEVEL2	100K	20K	682	0.3V	V1.1
LEVEL3	100K	51K	1365	0.6V	V1.2
LEVEL4	100K	100K	2047	0.9V	V4.0
LEVEL5	100K	200K	2730	1.2V	V5.0
LEVEL6	100K	499K	3412	1.5V	V6.0
LEVEL7	100K	DNP	4095	1.8V	V7.0

Namtso Technology Co., Ltd			
Project:	A10		
File:	RK3588_SARADC/1V8 GPIO		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	10

U1Q

MIPI D/C-PHY DSI_TX Port0

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C — AN26 — MIPI_DPHY0_TX_CLKP
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B — AP26 — MIPI_DPHY0_TX_CLKN
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B — AN24 — MIPI_DPHY0_TX_D0P
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A — AP24 — MIPI_DPHY0_TX_D0N
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A — AN25 — MIPI_DPHY0_TX_D1P
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C — AP25 — MIPI_DPHY0_TX_D1N
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B — AN27 — MIPI_DPHY0_TX_D2P
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A — AP27 — MIPI_DPHY0_TX_D2N
MIPI_DPHY0_TX_D3P/NO_USE_AN28 — AN28 — MIPI_DPHY0_TX_D3P
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C — AP28 — MIPI_DPHY0_TX_D3N

MIPI D/C-PHY CSI_RX Port0

D-PHY:V1.2 2.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

Note:
This D-PHY is limited!!!
Please refer to the
hardware design guide
for details.

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C — AN32 — MIPI_DPHY0_RX_CLKP
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B — AP31 — MIPI_DPHY0_RX_CLKN
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B — AN29 — MIPI_DPHY0_RX_D0P
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A — AP29 — MIPI_DPHY0_RX_D0N
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A — AN30 — MIPI_DPHY0_RX_D1P
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C — AP30 — MIPI_DPHY0_RX_D1N
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B — AN33 — MIPI_DPHY0_RX_D2P
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A — AP32 — MIPI_DPHY0_RX_D2N
MIPI_DPHY0_RX_D3P/NO_USE_AN34 — AN34 — MIPI_DPHY0_RX_D3P
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C — AP33 — MIPI_DPHY0_RX_D3N

MIPI D/C-PHY POWER

MIPI_D/C_PHY0_VREG — AF20 — C95 1uF C0201
MIPI_D/C_PHY0_VDD — AG20 — C84 100nF C0201, C90 1uF C0201 — VDD_0V75_S0
MIPI_D/C_PHY0_VDD_1V2 — AH20 — C78 1uF C0201 — VDDA_1V2_S0
MIPI_D/C_PHY0_VDD_1V8 — AJ20 — C71 1uF C0201 — VCC_1V8_S0

RK3588
BGA1088_23R00X23R00X2R00

U1R

MIPI D/C-PHY DSI_TX Port1

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C — AN20 — MIPI_DPHY1_TX_CLKP
MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B — AP20 — MIPI_DPHY1_TX_CLKN
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B — AN18 — MIPI_DPHY1_TX_D0P
MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A — AP18 — MIPI_DPHY1_TX_D0N
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A — AN19 — MIPI_DPHY1_TX_D1P
MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C — AP19 — MIPI_DPHY1_TX_D1N
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B — AN21 — MIPI_DPHY1_TX_D2P
MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A — AP21 — MIPI_DPHY1_TX_D2N
MIPI_DPHY1_TX_D3P/NO_USE_AN22 — AN22 — MIPI_DPHY1_TX_D3P
MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C — AP22 — MIPI_DPHY1_TX_D3N

MIPI D/C-PHY CSI_RX Port1

D-PHY:V1.2 2.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

Note:
This D-PHY is limited!!!
Please refer to the
hardware design guide
for details.

MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C — AK20 — MIPI_DPHY1_RX_CLKP
MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B — AL20 — MIPI_DPHY1_RX_CLKN
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B — AK18 — MIPI_DPHY1_RX_D0P
MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A — AL18 — MIPI_DPHY1_RX_D0N
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A — AK19 — MIPI_DPHY1_RX_D1P
MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C — AL19 — MIPI_DPHY1_RX_D1N
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B — AK21 — MIPI_DPHY1_RX_D2P
MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A — AL21 — MIPI_DPHY1_RX_D2N
MIPI_DPHY1_RX_D3P/NO_USE_AK22 — AK22 — MIPI_DPHY1_RX_D3P
MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C — AL22 — MIPI_DPHY1_RX_D3N

MIPI D/C-PHY POWER

MIPI_D/C_PHY1_VREG — AF19 — C97 1uF C0201
MIPI_D/C_PHY1_VDD — AG19 — C92 1uF C0201 — VDD_0V75_S0
MIPI_D/C_PHY1_VDD_1V2 — AH19 — C79 100nF C0201 — VDDA_1V2_S0
MIPI_D/C_PHY1_VDD_1V8 — AJ19 — C72 1uF C0201 — VCC_1V8_S0

RK3588
BGA1088_23R00X23R00X2R00

U1P

MIPI DPHY CSI_RX Port0

MIPI V1.2/2.5Gbps

MIPI_CSI0_CLK0P/MIPI_CSI0_CLK0N — AJ33/AJ34 — MIPI_CSI0_RX_CLK0P/MIPI_CSI0_RX_CLK0N
MIPI_CSI0_D0P/MIPI_CSI0_D0N — AG33/AG34 — MIPI_CSI0_RX_D0P/MIPI_CSI0_RX_D0N
MIPI_CSI0_D1P/MIPI_CSI0_D1N — AH33/AH34 — MIPI_CSI0_RX_D1P/MIPI_CSI0_RX_D1N
MIPI_CSI0_CLK1P/MIPI_CSI0_CLK1N — AM33/AM34
MIPI_CSI0_D2P/MIPI_CSI0_D2N — AK33/AK34 — MIPI_CSI0_RX_D2P/MIPI_CSI0_RX_D2N
MIPI_CSI0_D3P/MIPI_CSI0_D3N — AL33/AL34 — MIPI_CSI0_RX_D3P/MIPI_CSI0_RX_D3N
MIPI_CSI0_AVCC0V75 — AB25 — C83 100nF C0201, C143 1uF C0201 — VDD_0V75_S0
MIPI_CSI0_AVCC1V8 — AB26 — C138 1uF C0201 — VCC_1V8_S0

MIPI DPHY CSI_RX Port1

MIPI V1.2/2.5Gbps

MIPI_CSI1_CLK0P/MIPI_CSI1_CLK0N — AJ31/AJ32 — MIPI_CSI1_RX_CLK0P/MIPI_CSI1_RX_CLK0N
MIPI_CSI1_D0P/MIPI_CSI1_D0N — AG31/AG32 — MIPI_CSI1_RX_D0P/MIPI_CSI1_RX_D0N
MIPI_CSI1_D1P/MIPI_CSI1_D1N — AH31/AH32 — MIPI_CSI1_RX_D1P/MIPI_CSI1_RX_D1N
MIPI_CSI1_CLK1P/MIPI_CSI1_CLK1N — AM31/AM32
MIPI_CSI1_D2P/MIPI_CSI1_D2N — AK31/AK32 — MIPI_CSI1_RX_D2P/MIPI_CSI1_RX_D2N
MIPI_CSI1_D3P/MIPI_CSI1_D3N — AL31/AL32 — MIPI_CSI1_RX_D3P/MIPI_CSI1_RX_D3N
MIPI_CSI1_AVCC0V75 — AA25 — C96 1uF C0201 — VDD_0V75_S0
MIPI_CSI1_AVCC1V8 — AA26 — C144 100nF C0201 — VCC_1V8_S0

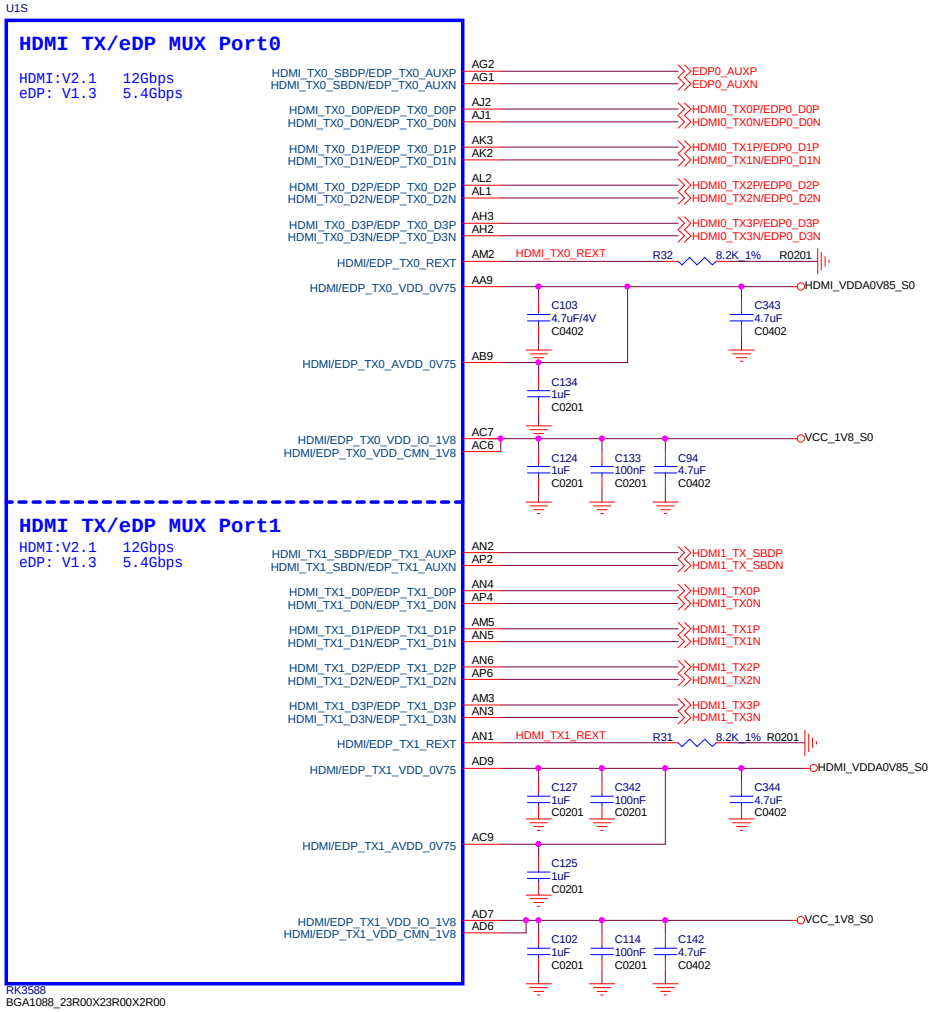
RK3588
BGA1088_23R00X23R00X2R00

MIPI_CSI_RX Configuration

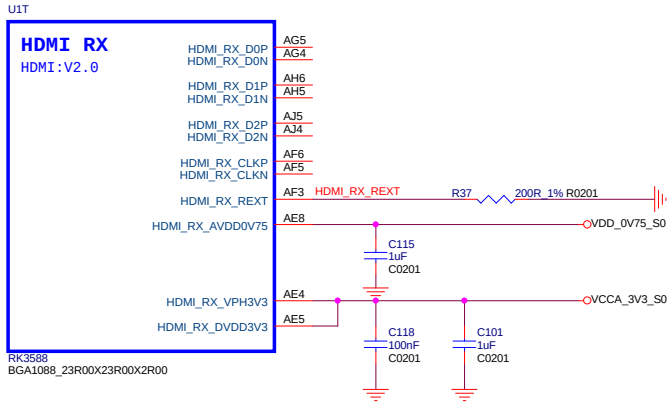
Option1	***Sensor1 x4Lane***	***MIPI_CSI_RX_D0-3*** ***MIPI_CSI_RX_CLK0***
Option2	***Sensor1 x2Lane*** ***+*** ***Sensor2 x2Lane***	***MIPI_CSI_RX_D0-1*** ***MIPI_CSI_RX_CLK0***
		MIPI_CSI_RX_D2-3 ***MIPI_CSI_RX_CLK1***

Namtso Technology Co., Ltd			
Project:	**A10**		
File:	**RK3588_MIPI Interface**		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	11

RK3588_S(HDMI2.1 TX)



RK3588_T(HDMI20 RX)



Namtso Technology Co., Ltd			
Project:	**A10**		
File:	RK3588_HDMI/EDP Interface		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	12

RK3588_N(PCIE20)

U1N

PCIE20/SATA30 Mux0

PCIe20x1_2
1Lane(RC)--4(1L2)

SATA30 HOST
Controller0

MUX

input or output

PCIE20_0_REFCLKP — L32 — PCIE20X1_2_REFCLKP
PCIE20_0_REFCLKN — L33 — PCIE20X1_2_REFCLKN
PCIE20_0_TXP/SATA30_0_TXP — M34 — PCIE20X1_2_TXP
PCIE20_0_TXN/SATA30_0_TXN — M33 — PCIE20X1_2_TXN
PCIE20_0_RXP/SATA30_0_RXP — N33 — PCIE20X1_2_RXP
PCIE20_0_RXN/SATA30_0_RXN — N34 — PCIE20X1_2_RXN
PCIE20_SATA30_0_AVDD_0V85 — M28 — VDDA_0V85_S0
C228 10uF C0402
PCIE20_SATA30_0_AVDD_1V8 — M27 — VCCA_1V8_S0
C223 1uF C0201

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30 Mux1

PCIe30x1_0
1Lane(RC)--2(1L0)

SATA30 HOST
Controller1

MUX

input or output

PCIE20_1_REFCLKP — H32 — PCIE30X1_0_REFCLKP
PCIE20_1_REFCLKN — H33 — PCIE30X1_0_REFCLKN
PCIE20_1_TXP/SATA30_1_TXP — K33 — PCIE30X1_0_TXP
PCIE20_1_TXN/SATA30_1_TXN — K34 — PCIE30X1_0_TXN
PCIE20_1_RXP/SATA30_1_RXP — J33 — PCIE30X1_0_RXP
PCIE20_1_RXN/SATA30_1_RXN — J34 — PCIE30X1_0_RXN
PCIE20_SATA30_1_AVDD_0V85 — L28 — VDDA_0V85_S0
C227 100nF C0201
PCIE20_SATA30_1_AVDD_1V8 — L27 — VCCA_1V8_S0
C210 100nF C0201

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30/USB30 HOST Mux2

PCIe30x1_1
1Lane(RC)--3(1L1)

SATA30 HOST
Controller2

USB30 HOST
Controller2

MUX

input or output

PCIE20_2_REFCLKP — G31
PCIE20_2_REFCLKN — G30
PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP — H30 — USB30_2_SSTXP
PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN — H29 — USB30_2_SSTXN
PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP — J31 — USB30_2_SSRXP
PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN — J30 — USB30_2_SSRXN
PCIE20_SATA30_USB30_2_AVDD_0V85 — K28 — VDDA_0V85_S0
C241 1uF C0201
PCIE20_SATA30_USB30_2_AVDD_1V8 — K27 — VCCA_1V8_S0
C229 1uF C0201

PCIE20:Gen1/Gen2
USB 30:Gen1
SATA30:Gen1/Gen2/Gen3

RK3588
BGA1088_23R00X23R00X2R00

RK3588_O(PCIE30)

U1O

PCIE30X4

PCIe30X4
4Lane(DM)--0(4L)

PCIe30x1_0
1Lane(RC)--2(1L0)

PCIE20/SATA30 MUX1

PCIE30:
PCIe1.1(2.5Gbps)
PCIe2.1(5Gbps)
PCIe3.0(8Gbps)

PCIe30x2
2Lane(RC)--1(2L)

PCIe30x1_1
1Lane(RC)--3(1L1)

PCIE20/SATA30/USB30 MUX2

PCIE30 PORT0

input

PCIE30_PORT0_REF_CLKP — E33 — PCIE30_PORT0_REFCLKP
PCIE30_PORT0_REF_CLKN — E34 — PCIE30_PORT0_REFCLKN

Lane0

PCIE30_PORT0_TX0P — D32 — PCIE30_PORT0_TX0P
PCIE30_PORT0_TX0N — D33 — PCIE30_PORT0_TX0N
PCIE30_PORT0_RX0P — G33 — PCIE30_PORT0_RX0P
PCIE30_PORT0_RX0N — G34 — PCIE30_PORT0_RX0N

Lane1

PCIE30_PORT0_TX1P — C33 — PCIE30_PORT0_TX1P
PCIE30_PORT0_TX1N — C34 — PCIE30_PORT0_TX1N
PCIE30_PORT0_RX1P — F32 — PCIE30_PORT0_RX1P
PCIE30_PORT0_RX1N — F33 — PCIE30_PORT0_RX1N

PCIE30_PORT0_RESREF — B34 — PCIE30_0_REF — R55 200R_1% R0201
PCIE30_PORT0_AVDD0V75 — G24 — VDD_0V75_S0
C259 1uF C0201
C272 4.7uF C0402
PCIE30_PORT0_AVDD1V8 — G23 — VCCA_1V8_S0
C258 1uF C0201
C59 4.7uF C0402

PCIE30 PORT1

input

PCIE30_PORT1_REF_CLKP — A28 — PCIE30_PORT1_REFCLKP
PCIE30_PORT1_REF_CLKN — B28 — PCIE30_PORT1_REFCLKN

Lane0

PCIE30_PORT1_TX0P — B30 — PCIE30_PORT1_TX2P
PCIE30_PORT1_TX0N — A30 — PCIE30_PORT1_TX2N
PCIE30_PORT1_RX0P — B32 — PCIE30_PORT1_RX2P
PCIE30_PORT1_RX0N — A32 — PCIE30_PORT1_RX2N

Lane1

PCIE30_PORT1_TX1P — C29 — PCIE30_PORT1_TX3P
PCIE30_PORT1_TX1N — B29 — PCIE30_PORT1_TX3N
PCIE30_PORT1_RX1P — C31 — PCIE30_PORT1_RX3P
PCIE30_PORT1_RX1N — B31 — PCIE30_PORT1_RX3N

PCIE30_PORT1_RESREF — A33 — PCIE30_1_REF — R56 200R_1% R0201
PCIE30_PORT1_AVDD0V75 — H24 — VDD_0V75_S0
C254 1uF C0201
C274 4.7uF C0402
PCIE30_PORT1_AVDD1V8 — H23 — VCCA_1V8_S0
C253 100nF C0201
C264 4.7uF C0402

RK3588
BGA1088_23R00X23R00X2R00

Namtso Technology Co., Ltd			
Project:	A10		
File:	RK3588_PCIE30/20		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	13

RK3588_J(VCCIO5 Domain)

U1J

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0	/ SPI4_MISO_M1	/	/ I2C6_SDA_M4	/ FSPI_D0_M2	/ I2S3_MCLK	/ SDIO_D0_M1	/ GMAC1_TXD2	/ GPIO3_A0_u	AA29
AUDDSM_LN	/ SPI4_MOSI_M1	/ PWM11_IR_M0	/ I2C6_SCL_M4	/ FSPI_D1_M2	/ I2S3_SCLK	/ SDIO_D1_M1	/ GMAC1_TXD3	/ GPIO3_A1_u	AA30
AUDDSM_LP	/ SPI4_CLK_M1	/ UART8_TX_M1	/	/ FSPI_D2_M2	/ I2S3_LRCK	/ SDIO_D2_M1	/ GMAC1_RXD2	/ GPIO3_A2_u	AD27
AUDDSM_RN	/ SPI4_CS0_M1	/ UART8_RX_M1	/	/ FSPI_D3_M2	/ I2S3_SDO	/ SDIO_D3_M1	/ GMAC1_RXD3	/ GPIO3_A3_u	AE27
AUDDSM_RP	/ SPI4_CS1_M1	/ UART8_RTSN_M1	/	/	/ I2S3_SDI	/ SDIO_CMD_M1	/ GMAC1_TXCLK	/ GPIO3_A4_d	AD28
	/ MIPI_CAMERA0_CLK_M1	/ UART8_CTSN_M1	/ I2C4_SDA_M0	/ FSPI_CLK_M2	/	/ SDIO_CLK_M1	/ GMAC1_RXCLK	/ GPIO3_A5_d	AH30
	/ MIPI_CAMERA1_CLK_M1	/	/ I2C4_SCL_M0	/	/	/	/ ETH1_REFCLKO_25M	/ GPIO3_A6_d	AH27
PWM8_M0	/ MIPI_CAMERA2_CLK_M1	/	/	/	/	/	/ GMAC1_RXD0	/ GPIO3_A7_u	AG29
PWM9_M0	/ MIPI_CAMERA3_CLK_M1	/	/	/	/	/	/ GMAC1_RXD1	/ GPIO3_B0_u	AG28
PWM2_M1	/ MIPI_CAMERA4_CLK_M1	/ UART2_TX_M2	/	/	/	/	/ GMAC1_RXDV_CRS	/ GPIO3_B1_d	AH29
PWM3_IR_M1	/	/ UART2_RX_M2	/	/	/ I2S2_SDI_M1	/	/ GMAC1_TXER	/ GPIO3_B2_d	AE28
	/	/ UART2_RTSN	/	/	/ I2S2_SDO_M1	/	/ GMAC1_TXD0	/ GPIO3_B3_u	AC28
	/	/ UART2_CTSN	/	/	/ I2S2_MCLK_M1	/	/ GMAC1_TXD1	/ GPIO3_B4_u	AC29
PWM12_M0	/ CAN1_RX_M0	/ UART3_TX_M1	/	/	/ I2S2_SCLK_M1	/	/ GMAC1_TXEN	/ GPIO3_B5_u	AD29
PWM13_M0	/ CAN1_TX_M0	/ UART3_RX_M1	/	/	/ I2S2_LRCK_M1	/	/ GMAC1_MCLKINOUT	/ GPIO3_B6_d	AE29
	/	/	/ I2C3_SCL_M1	/ SPI1_MOSI_M1	/ HDMI_TX1_HPD_M1	/	/ GMAC1_PTP_REF_CLK	/ GPIO3_B7_d	AA28
	/	/ UART7_TX_M1	/ I2C3_SDA_M1	/ SPI1_MISO_M1	/	/	/ GMAC1_PPSTRIG	/ GPIO3_C0_d	Y29
	/ PCIE30X2_BUTTON_RSTN	/ UART7_RX_M1	/	/ SPI1_CLK_M1	/	/	/ GMAC1_PPSCLK	/ GPIO3_C1_d	Y27
PWM14_M0	/	/ UART7_RTSN_M1	/ I2C8_SCL_M4	/ SPI1_CS0_M1	/	/ MIPI_TE0	/ GMAC1_MDC	/ GPIO3_C2_d	Y31
PWM15_IR_M0	/	/ UART7_CTSN_M1	/ I2C8_SDA_M4	/ SPI1_CS1_M1	/	/ MIPI_TE1	/ GMAC1_MDIO	/ GPIO3_C3_d	Y30
CAN2_RX_M0	/ PCIE30X4_CLKREQN_M2	/ UART5_TX_M1	/ FSPI_CS0N_M2	/ SPI3_CS0_M3	/ HDMI_TX1_CEC_M2	/	/ CIF_D8	/ GPIO3_C4_u	AH26
CAN2_TX_M0	/ PCIE30X4_WAKEN_M2	/ UART5_RX_M1	/ FSPI_CS1N_M2	/ SPI3_CS1_M3	/ HDMI_TX1_SDA_M1	/	/ CIF_D9	/ GPIO3_C5_u	AH25
	/ PCIE30X4_PERSTN_M2	/	/	/ SPI3_MISO_M3	/ HDMI_TX1_SCL_M1	/	/ CIF_D10	/ GPIO3_C6_u	AG26
	/ PCIE20X1_2_CLKREQN_M0	/	/ I2C5_SCL_M0	/ SPI3_MOSI_M3	/ HDMI_TX0_SCL_M2	/	/ CIF_D11	/ GPIO3_C7_u	AJ24
PWM8_M2	/ PCIE20X1_2_WAKEN_M0	/ UART4_RX_M1	/ I2C5_SDA_M0	/ SPI3_CLK_M3	/ HDMI_TX0_SDA_M2	/	/ CIF_D12	/ GPIO3_D0_u	AH24
PWM9_M2	/ PCIE20X1_2_PERSTN_M0	/ UART4_TX_M1	/	/ SPI0_MISO_M3	/ HDMI_RX_CEC_M1	/	/ CIF_D13	/ GPIO3_D1_d	AG23
	/ PCIE30X2_CLKREQN_M2	/ UART9_RTSN_M2	/ I2C7_SCL_M2	/ SPI0_MOSI_M3	/ HDMI_RX_SCL_M1	/	/ CIF_D14	/ GPIO3_D2_d	AG25
PWM10_M2	/ PCIE30X2_WAKEN_M2	/ UART9_CTSN_M2	/ I2C7_SDA_M2	/ SPI0_CLK_M3	/ HDMI_RX_SDA_M1	/	/ CIF_D15	/ GPIO3_D3_d	AG24
	/ PCIE30X2_PERSTN_M2	/ UART9_RX_M2	/	/ SPI0_CS0_M3	/ HDMI_RX_HPDOUT_M1	/ HDMI_TX0_HPD_M1	/ MCU_JTAG_TCK_M1	/ GPIO3_D4_d	AA27
PWM11_IR_M3	/ PCIE30X4_BUTTON_RSTN	/ UART9_TX_M2	/	/ SPI0_CS1_M3	/ DP1_HPDIN_M0	/	/ MCU_JTAG_TMS_M1	/ GPIO3_D5_d	AB28

VCCIO5_1V8

VCCIO5

RK3588
BGA1088_23R00X23R00X2R00

AA29 GMAC1_TXD2
AA30 GMAC1_TXD3
AD27 GMAC1_RXD2
AE27 GMAC1_RXD3
AD28 GMAC1_TXCLK
AH30 GMAC1_RXCLK
AH27 CH9434_INT_L
AG29 GMAC1_RXD0
AG28 GMAC1_RXD1
AH29 GMAC1_RXDV_CRS
AE28 SDMMC_PWREN
AC28 GMAC1_TXD0
AC29 GMAC1_TXD1
AD29 GMAC1_TXEN
AE29 LCD1_BL_PWM13_M0
AA28 LINK_GPIO3_B7_d
Y29 LCD1_PWREN_H
Y27 LCD1_RESET
Y31 GMAC1_MDC
Y30 GMAC1_MDIO
AH26 HDMITX1_CEC_M2
AH25 HDMITX1_SDA_M1
AG26 HDMITX1_SCL_M1
AJ24 EXT_GPIO3_C7_u
AH24 EXT_GPIO3_D0_u
AG23 PCIE20X1_2_PERSTN_M0
AG25 LCD2_PWREN_H
AG24 LCD2_BL_PWM10_M2
AA27 LCD2_RESET
AB28 DP1_HPDIN_M0

W25 — C109 100nF C0201 — VCC_1V8_S0

W26 — C157 100nF C0201 — VCCIO5_S0

VCCIO5_S0 — FB27 120R/100M FB0402 — EVDDIO

VCCIO5_S0 — FB28 DNP 120R/100M FB0402 — VCC_3V3_S0

Namtso Technology Co., Ltd			
Project:	A10		
File:	RK3588_GMAC IO		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	14

RK3588_I(VCCIO4 Domain)

U1I

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

		/SPI4_MISO_M2	/PCIE30X1_1_CLKREQN_M2	/ DP0_HPDIN_M2	/ I2C2_SDA_M4	/ UART6_RX_M1	/GPIO1_A0_d
SATA1_ACT_LED_M1 /		/	/SPI4_MOSI_M2	/PCIE30X1_1_WAKEN_M2	/ DP1_HPDIN_M2	/ I2C2_SCL_M4	/ UART6_TX_M1	/GPIO1_A1_d
		/ PWM0_M2	/SPI4_CLK_M2	/	/ VOP_POST_EMPTY	/ I2C4_SDA_M3	/ UART6_RTSN_M1	/GPIO1_A2_d
		/ PWM1_M2	/SPI4_CS0_M2	/	/ HDMI_TX1_SDA_M2	/ I2C4_SCL_M3	/ UART6_CTSN_M1	/GPIO1_A3_d
		/	/SPI2_MISO_M0	/	/ HDMI_TX1_SCL_M2	/	/	/GPIO1_A4_d
		/	/SPI2_MOSI_M0		/ HDMI_TX0_HPD_M0	/	/	/GPIO1_A5_d
		/	/SPI2_CLK_M0	/	/ HDMI_TX1_HPD_M0	/	/	/GPIO1_A6_d
		/ PWM3_IR_M3	/SPI2_CS0_M0	/PCIE30X1_1_PERSTN_M2	/	/ PDM1_SDI0_M1	/	/GPIO1_A7_u
		/	/SPI2_CS1_M0	/PCIE30X4_CLKREQN_M3	/	/ PDM1_SDI1_M1	/	/GPIO1_B0_u
		/	/SPI0_MISO_M2	/PCIE30X4_WAKEN_M3	/	/ PDM1_SDI2_M1	/	/GPIO1_B1_d
		/	/SPI0_MOSI_M2	/PCIE30X4_PERSTN_M3	/	/ PDM1_SDI3_M1	/ UART4_RX_M2	/GPIO1_B2_d
SATA0_ACT_LED_M1 /		/	/SPI0_CLK_M2	/PCIE30X1_0_WAKEN_M2	/	/ PDM1_CLK1_M1	/ UART4_TX_M2	/GPIO1_B3_d
		/	/SPI0_CS0_M2	/PCIE30X1_0_PERSTN_M2	/	/ PDM1_CLK0_M1	/ UART7_RX_M2	/GPIO1_B4_u
		/	/SPI0_CS1_M2	/PCIE30X1_0_CLKREQN_M2	/	/	/ UART7_TX_M2	/GPIO1_B5_u
	HDMI_RX_HPDOUT_M2 /		/SPDIF0_TX_M0	/PCIE30X2_WAKEN_M3	/ MIPI_CAMERA1_CLK_M0	/ I2C5_SCL_M3	/ UART1_TX_M1	/GPIO1_B6_u
SATA2_ACT_LED_M1 /	HDMI_RX_CEC_M2	/ PWM13_M2	/SPDIF1_TX_M0	/PCIE30X2_PERSTN_M3	/ MIPI_CAMERA2_CLK_M0	/ I2C5_SDA_M3	/ UART1_RX_M1	/GPIO1_B7_u
	HDMI_RX_SCL_M2	/ PWM14_M2	/	/	/ MIPI_CAMERA3_CLK_M0	/ I2C8_SCL_M2	/ UART1_RTSN_M1	/GPIO1_D6_u
	HDMI_RX_SDA_M2	/ PWM15_IR_M3	/	/PCIE30X2_CLKREQN_M3	/ MIPI_CAMERA4_CLK_M0	/ I2C8_SDA_M2	/ UART1_CTSN_M1	/GPIO1_D7_u

A24	I2C2_SDA_M4			
A25	I2C2_SCL_M4			
A26	I2C4_SDA_M3			
A27	I2C4_SCL_M3			
B25	CAM2_PDN			
B26	HDMITX0_HPDIN_M0			
C24	HDMITX1_HPDIN_M0			
C25	CAM2_RST			
C27	CAM1_RST			
D25	CAM1_PDN			
D26	CAM3_PDN			
D27	GPIO1_B3_d			
E24	PCIE30X1_0_PERSTN_M2			
E25	GPIO1_B5_u			
E26	MIPI_CAM1_CLK	R57	0R R0402	CAM1_MCLK
E27	MIPI_CAM2_CLK	R58	0R R0402	CAM2_MCLK
F24	MIPI_CAM3_CLK	R59	0R R0402	CAM3_MCLK
F25	MIPI_CAM4_CLK	R60	0R R0402	CAM4_MCLK
H20	VCCIO4_1V8	C252 100nF C0201		VCC_1V8_S0
H21	VCCIO4			

VCC_1V8_S0

R12 2.2K R0402 — I2C2_SDA_M4

R13 2.2K R0402 — I2C2_SCL_M4

VCC_1V8_S0

R14 2.2K R0402 — I2C4_SDA_M3

R15 2.2K R0402 — I2C4_SCL_M3

GPIO1_B3_d	R89	DNP 0R R0402	PCIE30X1_0_WAKEN_M2	
GPIO1_B5_u	R90	DNP 0R R0402	PCIE30X1_0_CLKREQN_M2	
	R91	0R R0402	CAM3_RST	
	R92	0R R0402	CAM4_RST	

RK3588
BGA1088_23R00X23R00X2R00

RK3588_K(VCCIO6 Domain)

U1K

VCCIO6 Domain

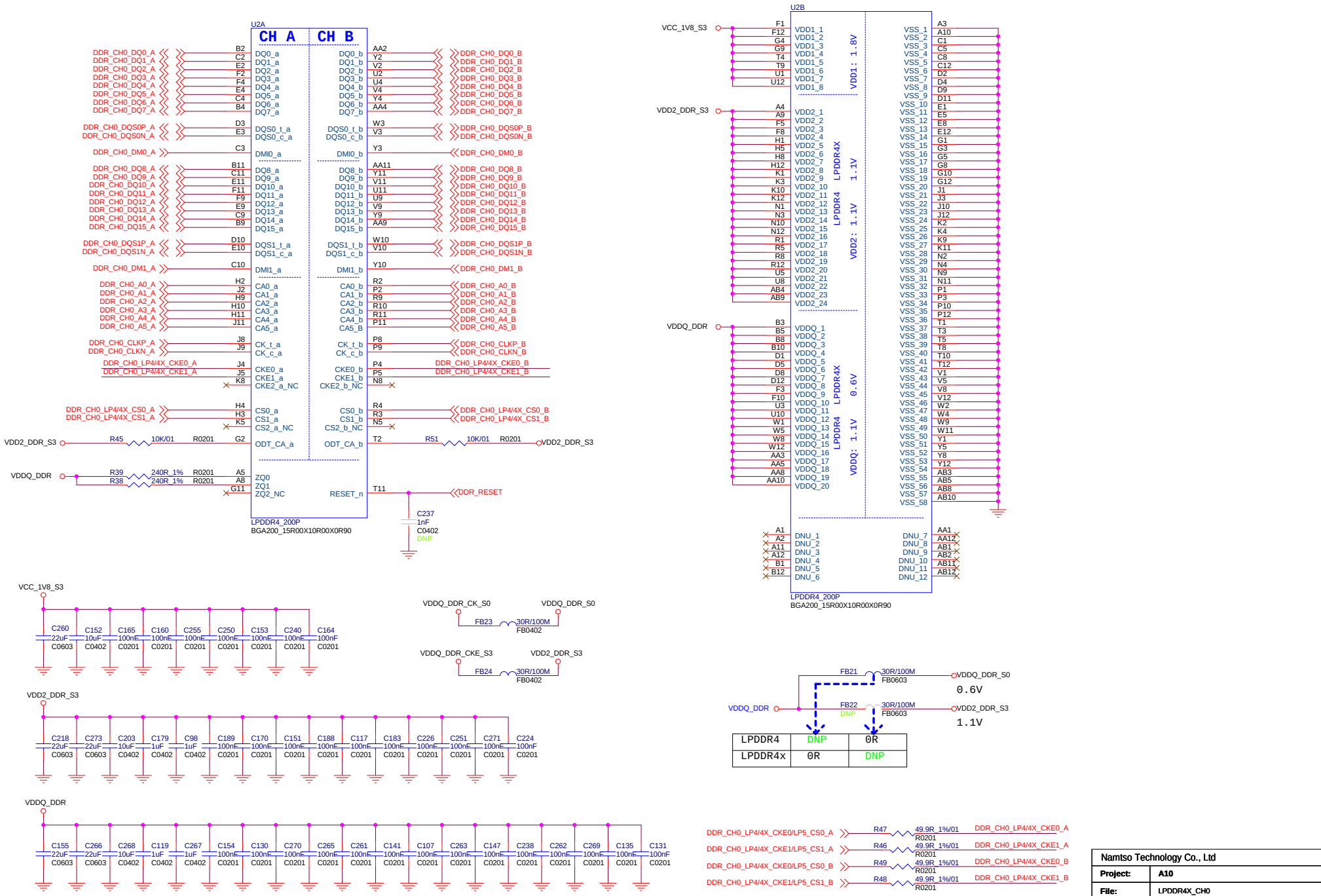
Operating Voltage=1.8V/3.3V

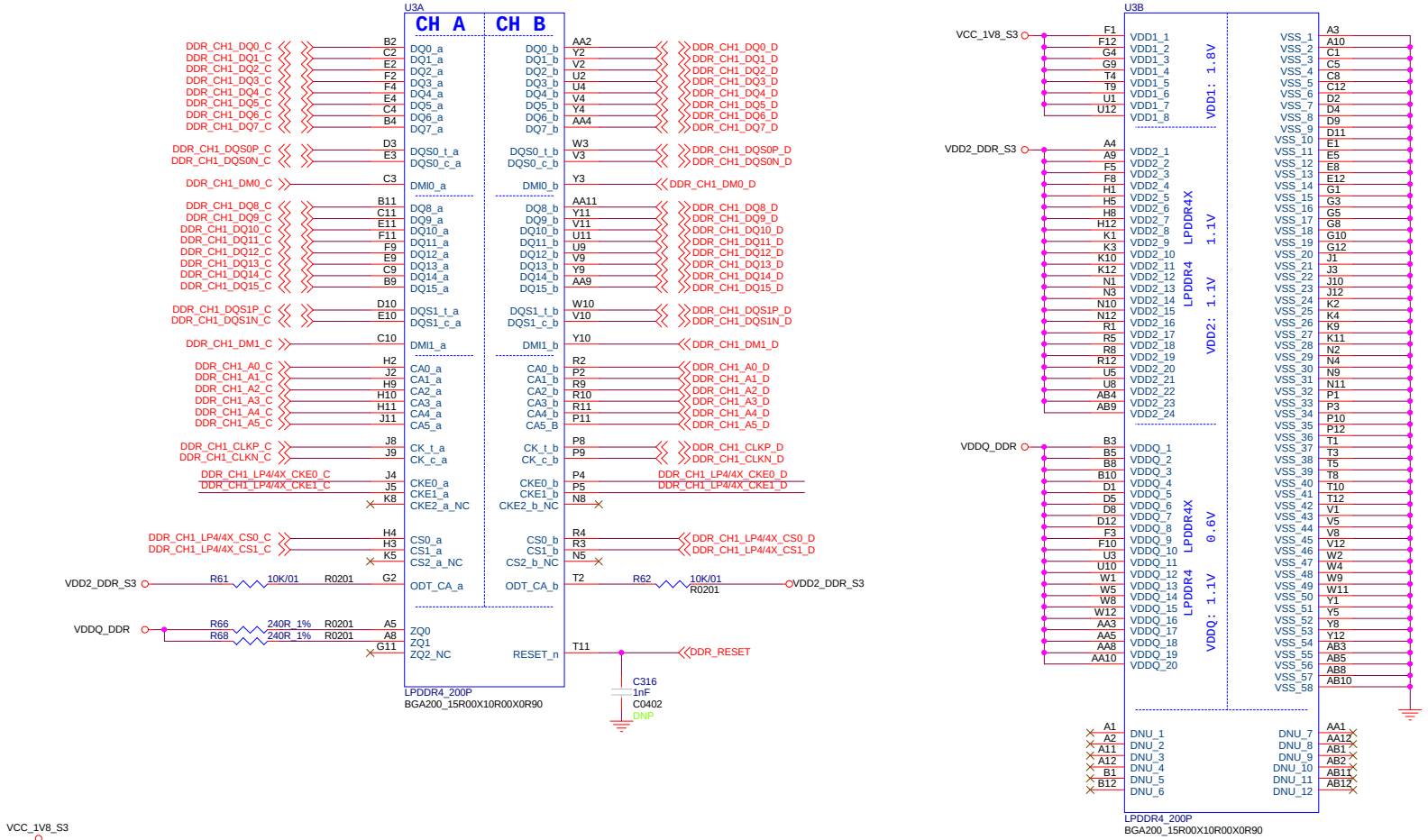
	/ SPI0_MISO_M1	/ UART9_RTSN_M1 /		/ I2S1_MCLK_M0	/ PCIE30X1_1_CLKREQN_M1	/ BT1120_D0	/ CIF_D0	/ GPIO4_A0_d
	/ SPI0_MOSI_M1	/ UART9_CTSN_M1 /		/ I2S1_SCLK_M0	/ PCIE30X1_1_WAKEN_M1	/ BT1120_D1	/ CIF_D1	/ GPIO4_A1_d
	/ SPI0_CLK_M1	/		/ I2S1_LRCK_M0	/ PCIE30X1_1_PERSTN_M1	/ BT1120_D2	/ CIF_D2	/ GPIO4_A2_d
	/	UART0_TX_M2	/	/	/ PCIE30X1_0_CLKREQN_M1	/ BT1120_D3	/ CIF_D3	/ GPIO4_A3_d
	/ SPI2_MISO_M1	/ UART0_RX_M2	/ I2C3_SCL_M2	/	/ PCIE30X1_0_WAKEN_M1	/ BT1120_D4	/ CIF_D4	/ GPIO4_A4_d
	/ SPI2_MOSI_M1	/ UART3_TX_M2	/ I2C3_SDA_M2	/ I2S1_SDI0_M0	/ PCIE30X1_0_PERSTN_M1	/ BT1120_D5	/ CIF_D5	/ GPIO4_A5_d
	/ SPI2_CLK_M1	/ UART3_RX_M2	/ I2C5_SCL_M2	/ I2S1_SDI1_M0	/ PCIE30X2_CLKREQN_M1	/ BT1120_D6	/ CIF_D6	/ GPIO4_A6_d
	/ SPI2_CS0_M1	/	/ I2C5_SDA_M2	/ I2S1_SDI2_M0	/ PCIE30X2_WAKEN_M1	/ BT1120_D7	/ CIF_D7	/ GPIO4_A7_d
	/ SPI2_CS1_M1	/ UART8_TX_M0	/ I2C6_SDA_M3	/ I2S1_SDI3_M0	/ PCIE30X2_PERSTN_M1	/ BT1120_CLKOUT	/ CIF_CLKIN	/ GPIO4_B0_d
SATA2_ACT_LED_M0 / SPDIF1_TX_M1	/ SPI0_CS1_M1	/ UART8_RX_M0	/ I2C6_SCL_M3	/ I2S1_SDO0_M0	/ PCIE30X1_0_BUTTON_RSTN	/	/ MIPI_CAMERA0_CLK_M0	/ GPIO4_B1_u
CAN1_RX_M1 / PWM14_M1	/ SPI0_CS0_M1	/ UART8_RTSN_M0	/ I2C7_SCL_M3	/ I2S1_SDO1_M0	/ PCIE30X1_1_BUTTON_RSTN	/ BT1120_D8	/ CIF_HREF	/ GPIO4_B2_u
CAN1_TX_M1 / PWM15_IR_M1	/	/ UART8_CTSN_M0	/ I2C7_SDA_M3	/ I2S1_SDO2_M0	/ PCIE20X1_2_BUTTON_RSTN	/ BT1120_D9	/ CIF_VSYNC	/ GPIO4_B3_u
SPDIF0_TX_M1 / PWM11_IR_M1	/ DP0_HPDIN_M0	/ UART9_TX_M1	/	/ I2S1_SDO3_M0	/ PCIE30X4_CLKREQN_M1	/ BT1120_D10	/ CIF_CLKOUT	/ GPIO4_B4_u
SATA1_ACT_LED_M0 / PWM12_M1	/ SPI3_MISO_M1	/ UART9_RX_M1	/	/HDMI_RX_CEC_M0	/ PCIE30X4_WAKEN_M1	/ BT1120_D11	/	/ GPIO4_B5_d
SATA0_ACT_LED_M0 / PWM13_M1	/ SPI3_MOSI_M1	/	/ I2C5_SCL_M1	/HDMI_RX_HPDOUT_M0	/ PCIE30X4_PERSTN_M1	/ BT1120_D12	/	/ GPIO4_B6_d
/	/ SPI3_CLK_M1	/	/ I2C5_SDA_M1	/HDMI_TX0_SCL_M0	/ PCIE20X1_2_CLKREQN_M1	/ BT1120_D13	/	/ GPIO4_B7_u
	/ SPI3_CS0_M1	/	/ I2C8_SCL_M3	/HDMI_TX0_SDA_M0	/ PCIE20X1_2_WAKEN_M1	/ BT1120_D14	/	/ GPIO4_C0_u
SPDIF1_TX_M2 / PWM6_M1	/ SPI3_CS1_M1	/	/ I2C8_SDA_M3	/HDMI_TX0_CEC_M0	/ PCIE20X1_2_PERSTN_M1	/ BT1120_D15	/	/ GPIO4_C1_d

AK30	IO-Board_PWREN		
AL30	TO_MCU_RST_H		
AM29	TYPEC0_SBU1_DC		
AL29	TYPEC0_SBU2_DC		
AL28	RST_HOLD		
AK27	HDMI/EDP_SW		
AL27	VCC_5V0_EN		
AM27	CPU_SPI/BT_SW		
AK26	TO_MCU_BOOT_H		
AL24	HDMI1_TX_ON_H		
AK25	CAN1_RX_M1		
AM25	CAN1_TX_M1		
AL26	PCIE30X4_CLKREQn_M1_L		
AJ26	PCIE30X4_WAKEn_M1_L		
AJ27	PCIE30X4_PERSTn_M1_L		
AJ28	HDMITX0_SCL_M0		
AJ25	HDMITX0_SDA_M0		
AK24	HDMITX0_CEC_M0		
AC25	VCCIO6_1V8	C129 100nF C0201	VCC_1V8_S0
AC26	VCCIO6	C110 100nF C0201	VCC_3V3_S0

RK3588
BGA1088_23R00X23R00X2R00

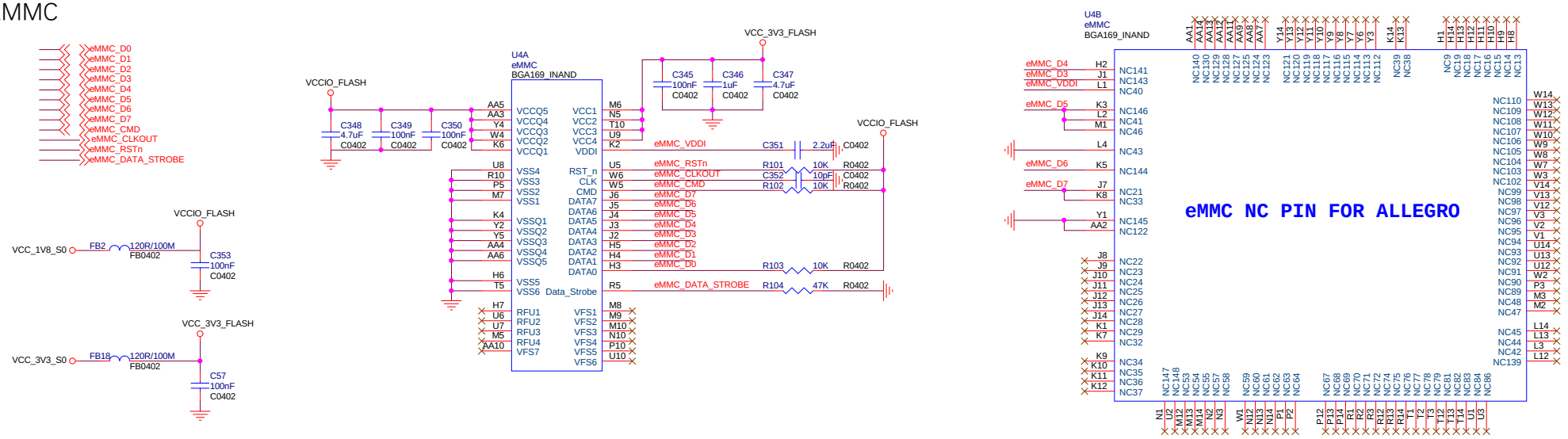
Namtso Technology Co., Ltd			
Project:	**A10**		
File:	**RK3588_1V8/3V3 GPIO**		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	15


U2A
CH A
CH B
LPDDR4_200P
BGA200_15R00X10R00X0R90
U2B
LPDDR4_200P
BGA200_15R00X10R00X0R90
VDD1: 1.8V
VDD2: 1.1V
VDDQ: 1.1V
LPDDR4 LPDDR4X
LPDDR4 0.6V
VCC_1V8_S3
VDD2_DDR_S3
VDDQ_DDR
VDDQ_DDR_CK_S0
VDDQ_DDR_S0
VDDQ_DDR_CKE_S3
VDD2_DDR_S3
FB23 30R/100M FB0402
FB24 30R/100M FB0402
FB21 30R/100M FB0603
FB22 DNP 30R/100M FB0603
0.6V
1.1V
DDR_RESET
C237 1nF C0402 DNP
R45 10K/01 R0201
R51 10K/01 R0201
R39 240R_1% R0201
R38 240R_1% R0201
R47 49.9R_1%/01 R0201
R46 49.9R_1%/01 R0201
R49 49.9R_1%/01 R0201
R48 49.9R_1%/01 R0201
DDR_CH0_LP4/4X_CKE0/LP5_CS0_A
DDR_CH0_LP4/4X_CKE1/LP5_CS1_A
DDR_CH0_LP4/4X_CKE0/LP5_CS0_B
DDR_CH0_LP4/4X_CKE1/LP5_CS1_B
DDR_CH0_LP4/4X_CKE0_A
DDR_CH0_LP4/4X_CKE1_A
DDR_CH0_LP4/4X_CKE0_B
DDR_CH0_LP4/4X_CKE1_B
LPDDR4 DNP 0R
LPDDR4x 0R DNP
Namtso Technology Co., Ltd
Project: A10
File: LPDDR4X_CH0
Date: Wednesday, January 24, 2024
Rev: V12
Designed_by: Totti Liang
Sheet: 16

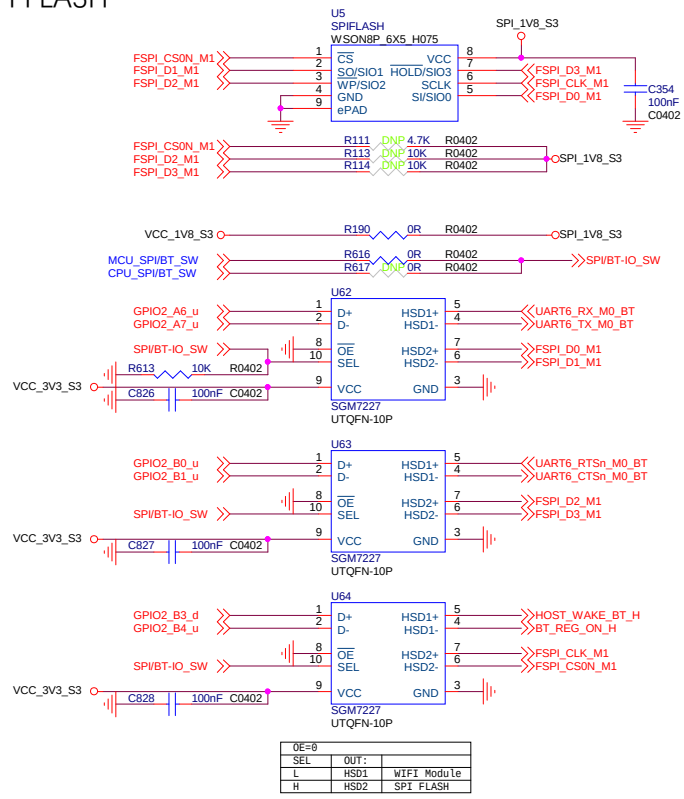


Namtso Technology Co., Ltd			
Project:	A10		
File:	LPDDR4X_CH1		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	17

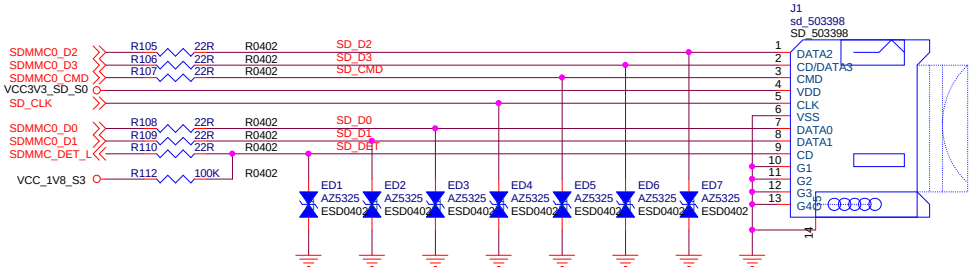
EMMC



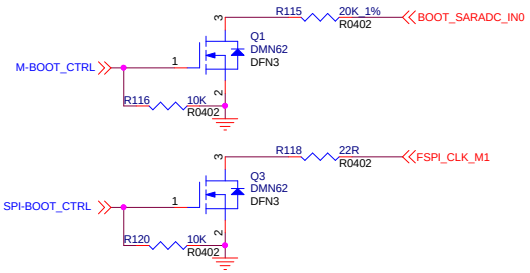
SPI FLASH



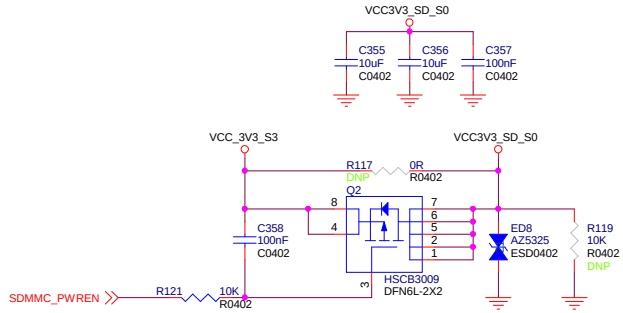
TF CARD



TST Ctrl

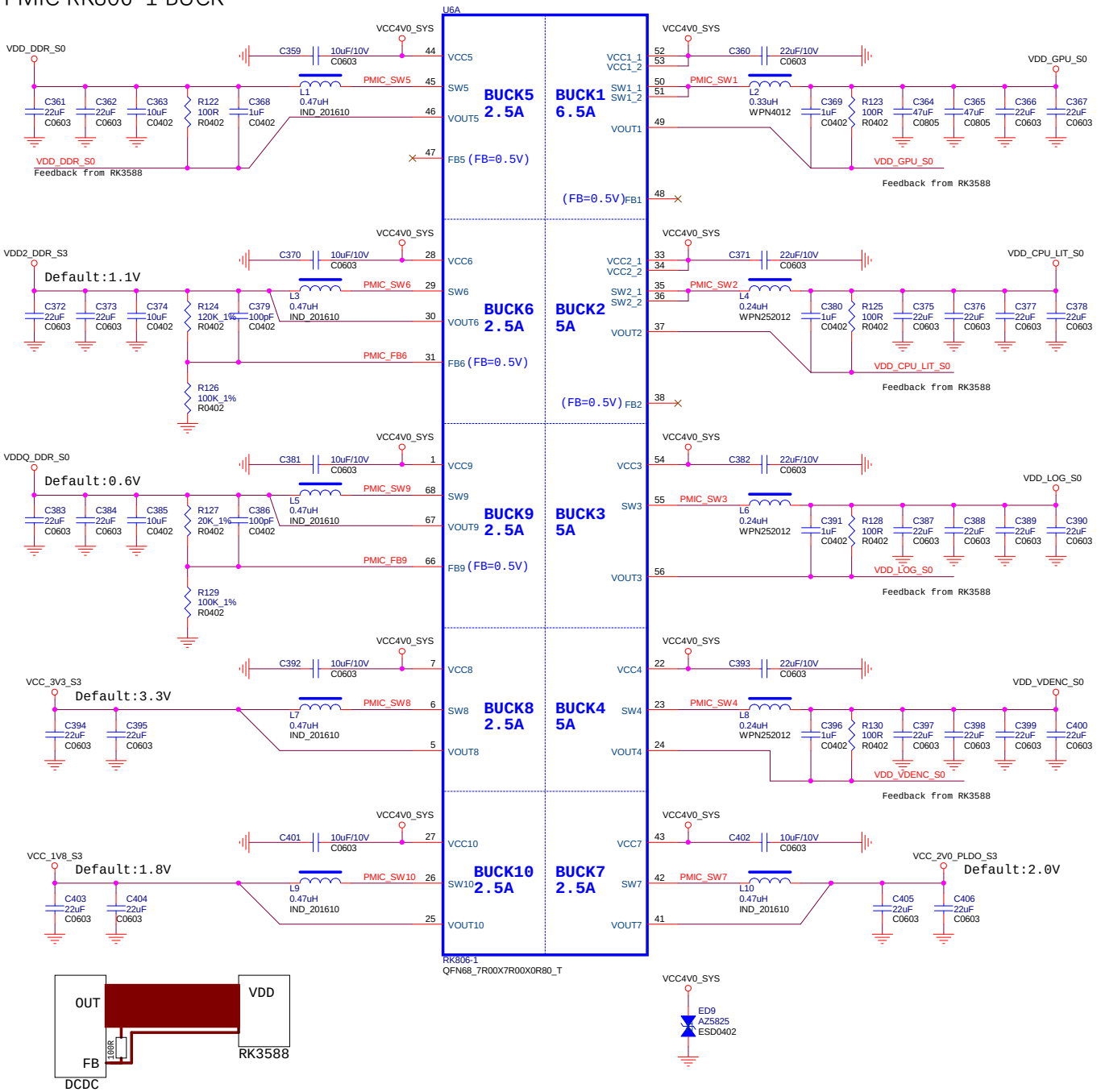


M-BOOT_CTRL	SPI-BOOT_CTRL	BOOT Priority
L	H	EMMC>USB
H	X	SD>USB
L	L	SPI>EMMC>USB default

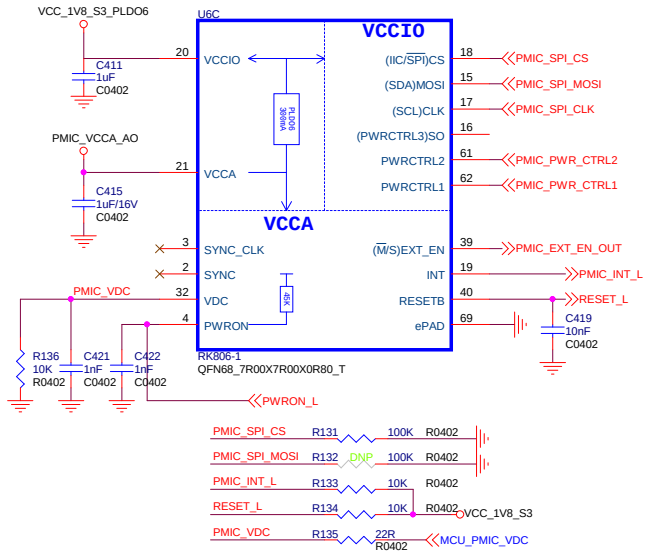


Namtso Technology Co., Ltd			
Project:	A10		
File:	EMMC/SPI-FLASH/TF		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	18

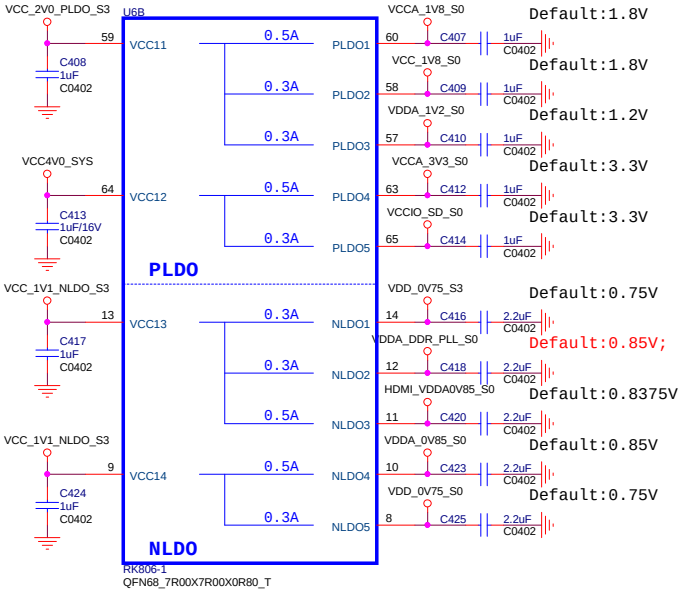
PMIC RK806-1 BUCK



PMIC RK806-1 Managerment

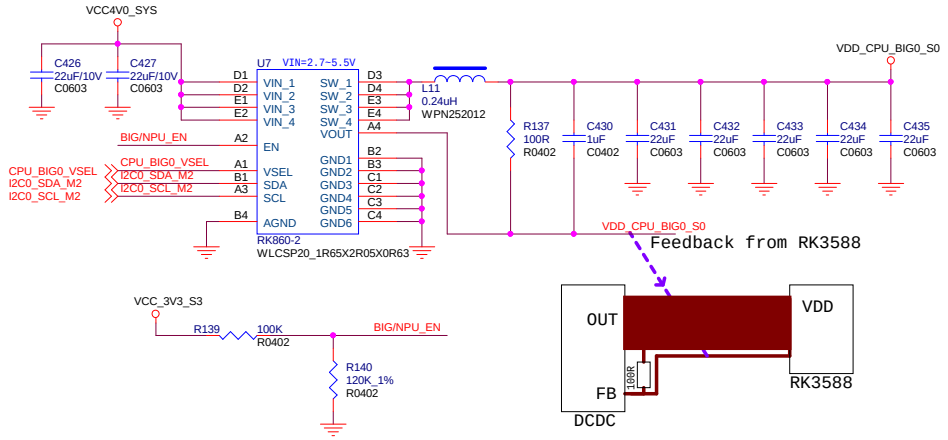


PMIC RK806-1 LDO

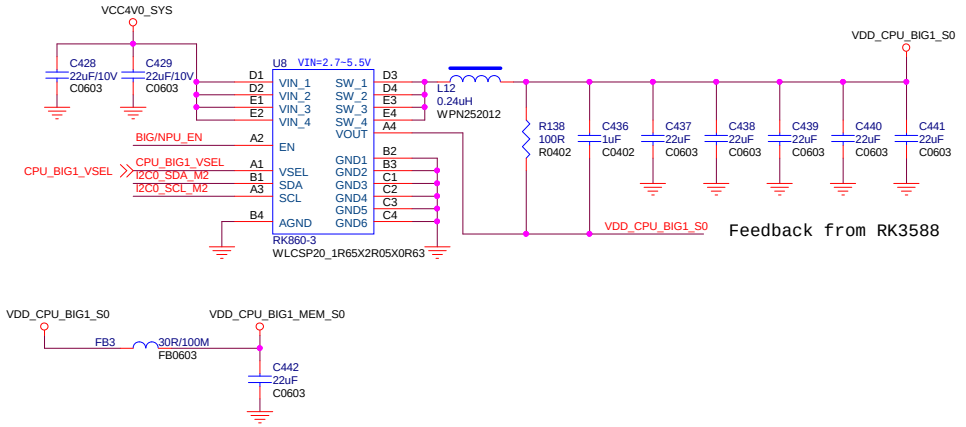


Namtso Technology Co., Ltd			
Project:	A10		
File:	Power_PMIC		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	19

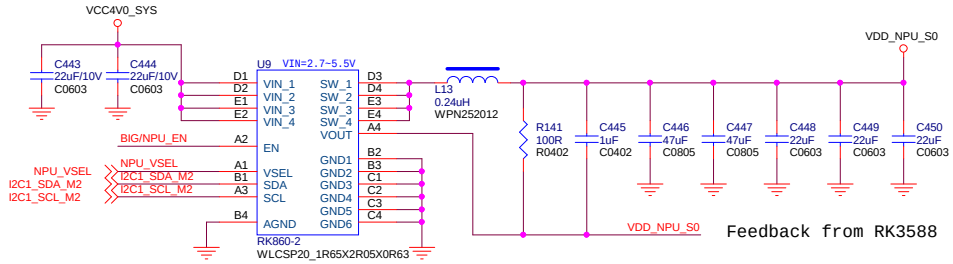
VDD_CPU_BIG0



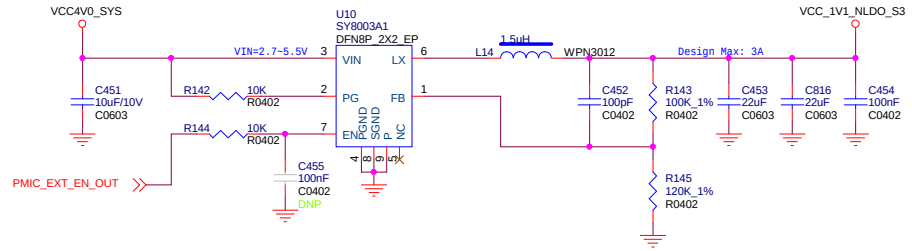
VDD_CPU_BIG1



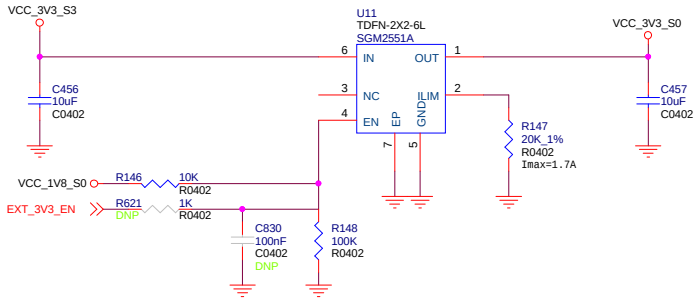
VDD_NPU



VCC_1V1_NLDO_S3

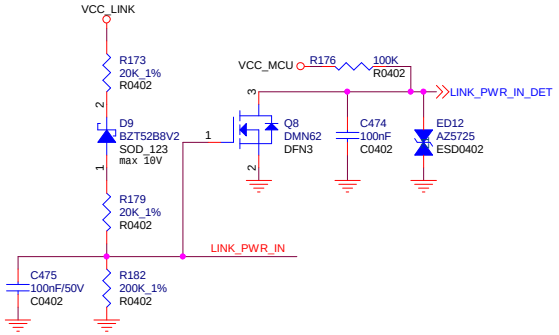


VCC_3V3_S0

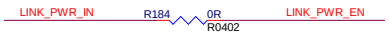


Namtso Technology Co., Ltd			
Project:	**A10**		
File:	Power_Ext Discrete		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	20

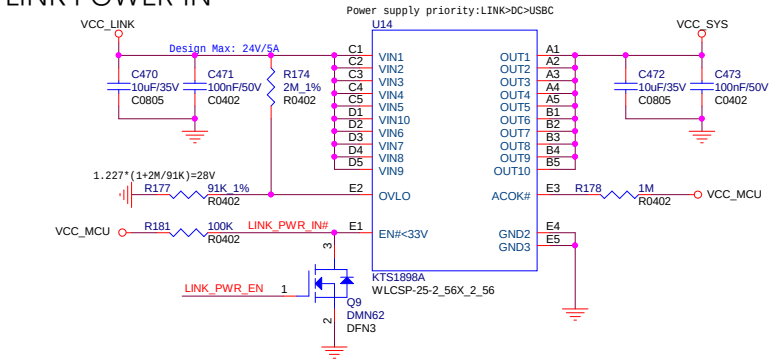
LINK PWR_DET



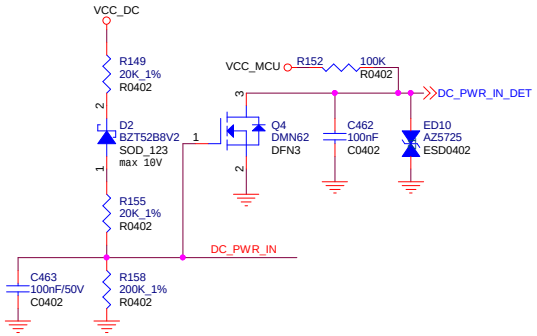
PWR Priority



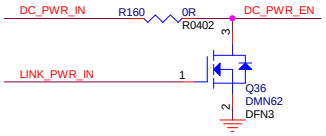
LINK POWER IN



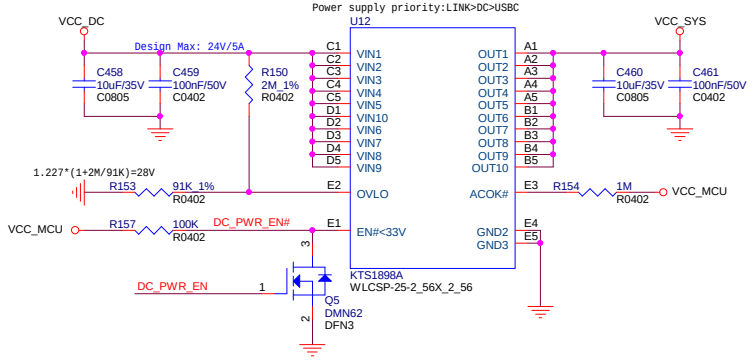
DC PWR_DET



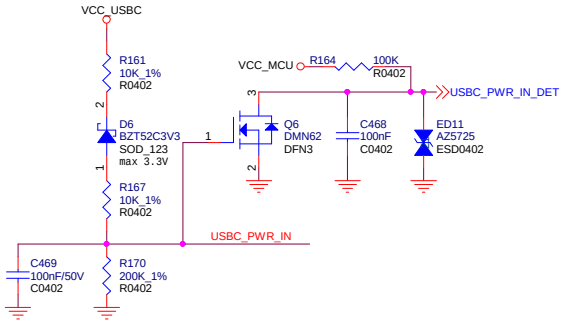
PWR Priority



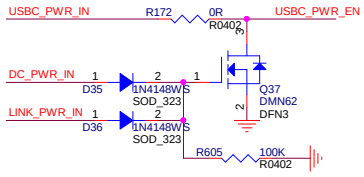
DC POWER IN



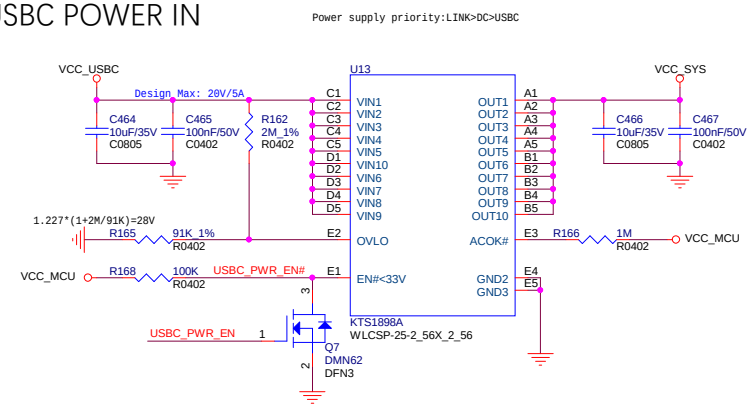
USBC PWR_DET



PWR Priority

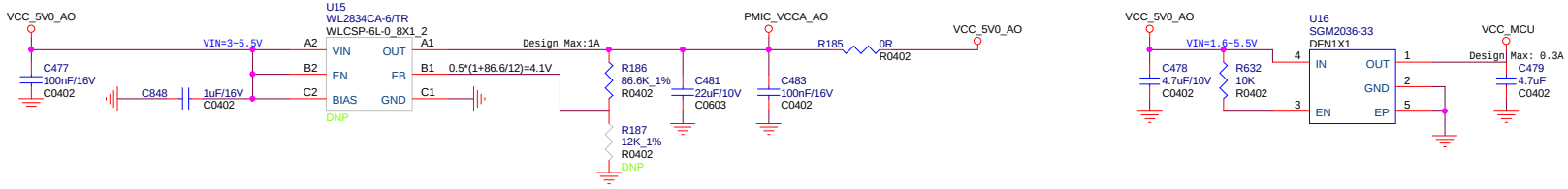


USBC POWER IN

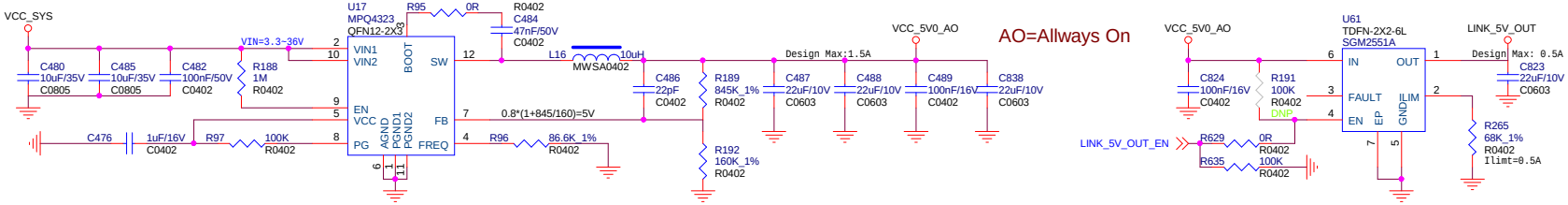


Namtso Technology Co., Ltd			
Project:	**A10**		
File:	**Power_Path**		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	21

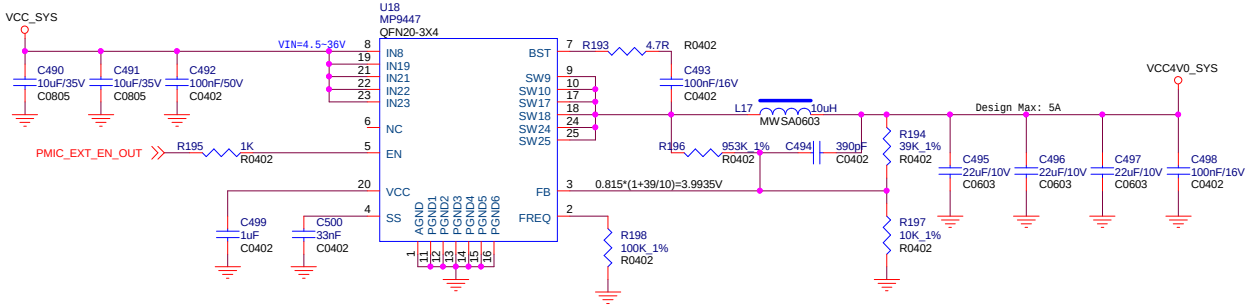
VCC_MCU



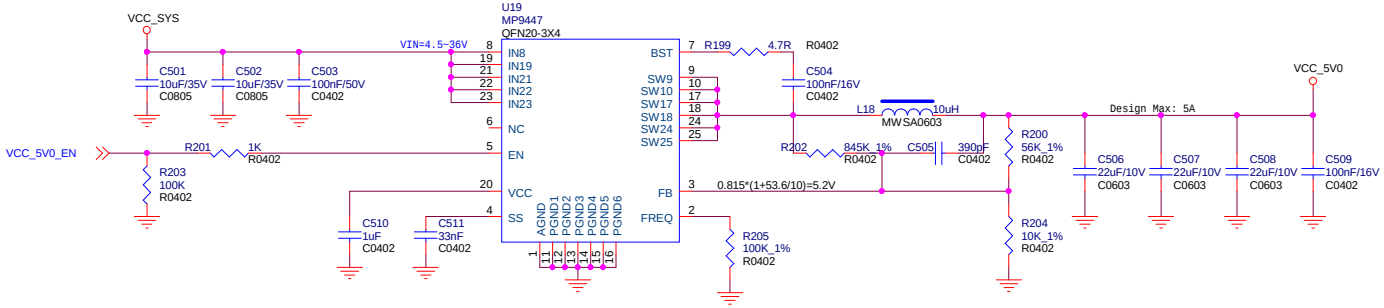
LINK_5V_OUT



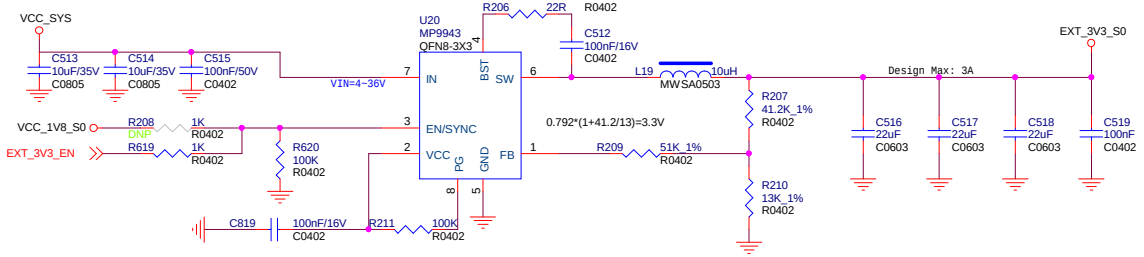
VCC4V0_SYS



VCC_5V0

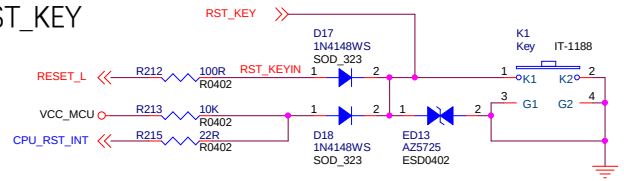


EXT_3V3_S0

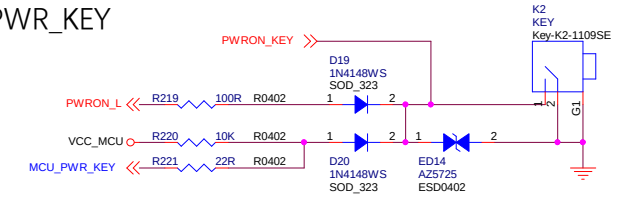


Namtso Technology Co., Ltd			
Project:	**A10**		
File:	**Power_5V/4V/3V3**		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	22

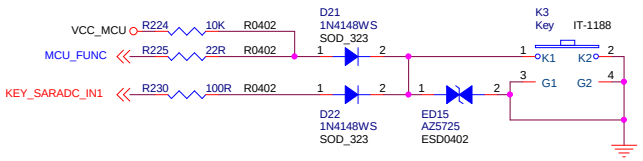
RST_KEY



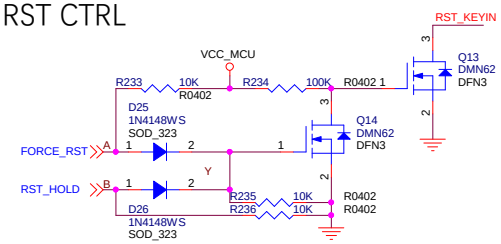
PWR_KEY



FUNCTION_KEY

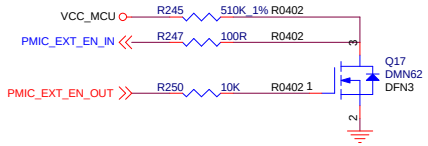


CPU RST CTRL

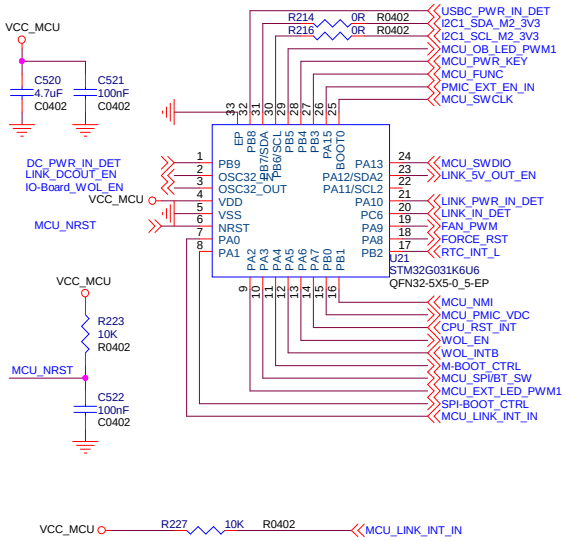


A	B	Y	RST_KEYIN
H	L	H	H (default)
X	H	H	H (MCU Update)
L	L	L	L (CPU RST)

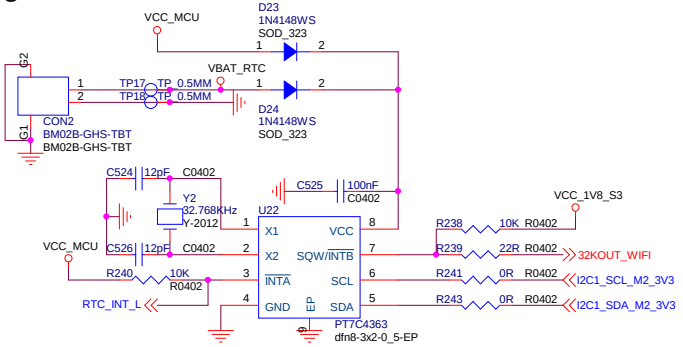
POWER OFF DET



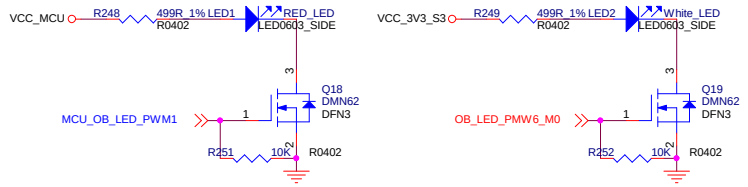
MCU



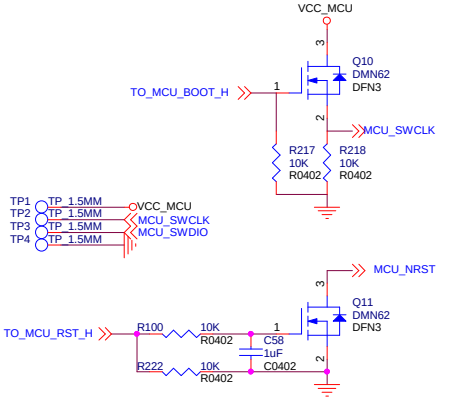
RTC



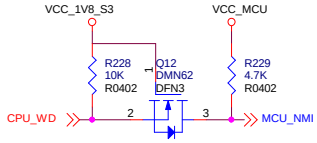
On Board_LED



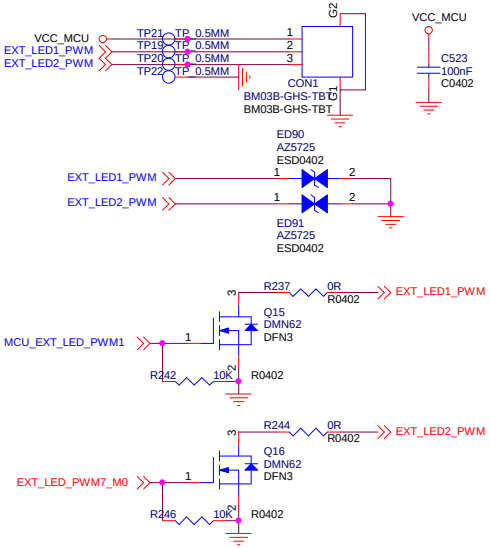
MCU BOOT CTRL



WATCH DOG

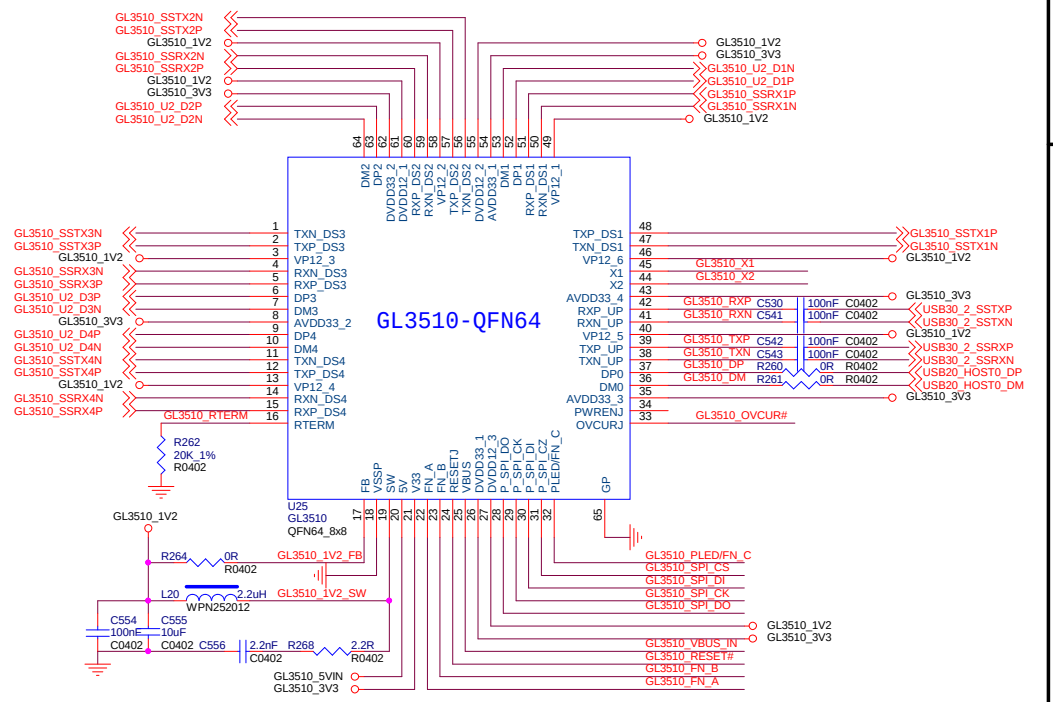


EXT_LED

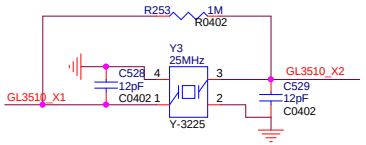


Namtso Technology Co., Ltd			
Project:	A10		
File:	MCU/RTC/KEY		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	23

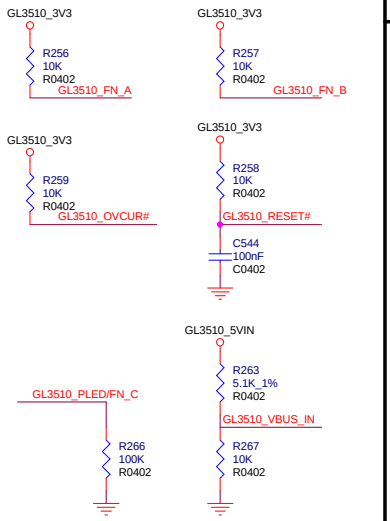
USB30 HUB



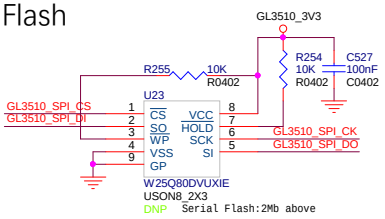
OSC



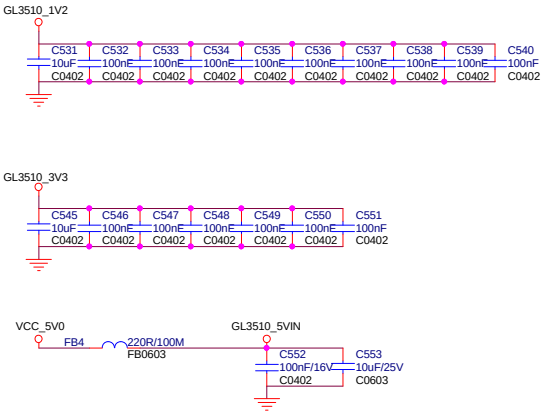
Config



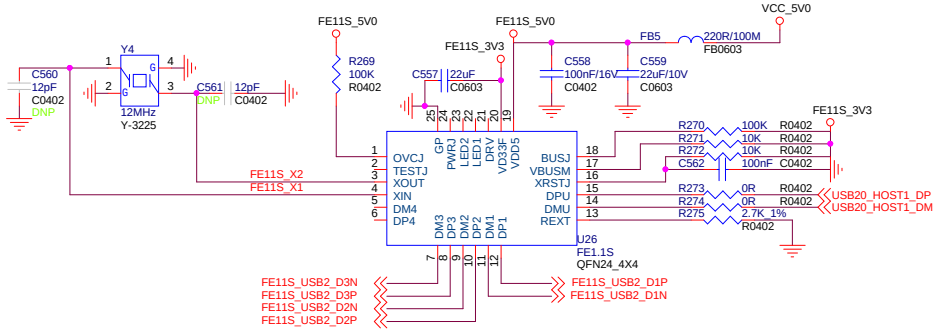
SPI Flash



Filter

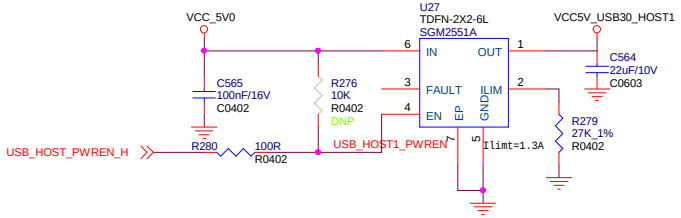


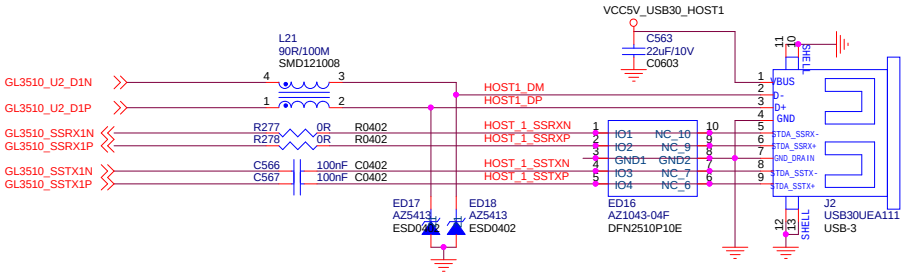
USB20 HUB



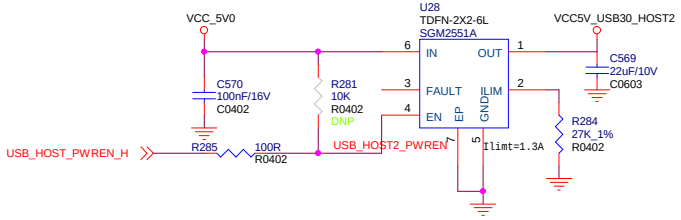
Namtso Technology Co., Ltd			
Project:	**A10**		
File:	**USB HUB**		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	24

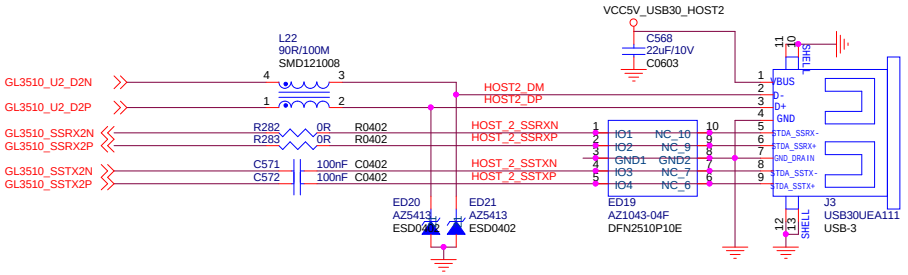
USB30 HOST1



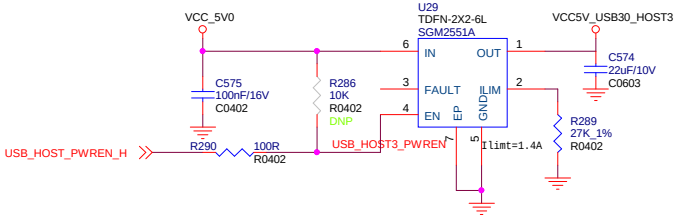


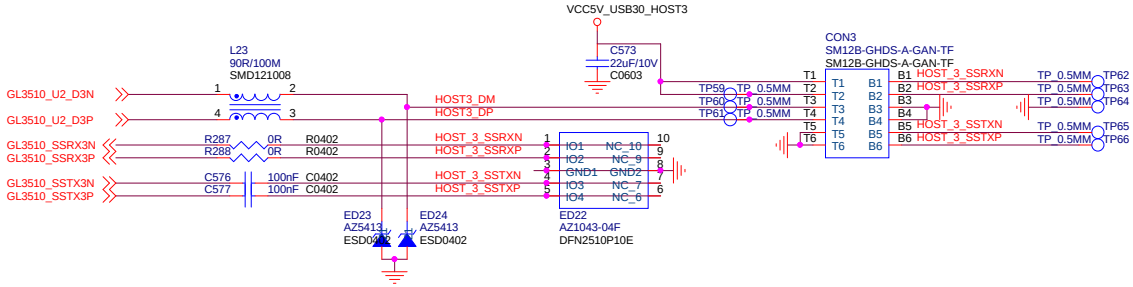
USB30 HOST2



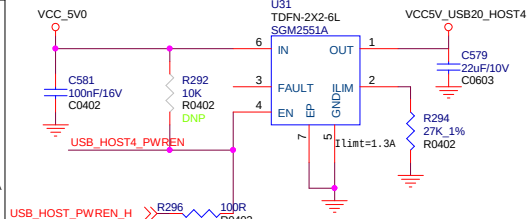


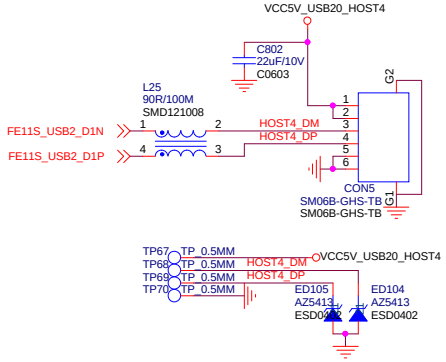
USB30 HOST3



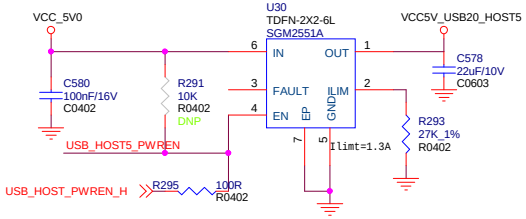


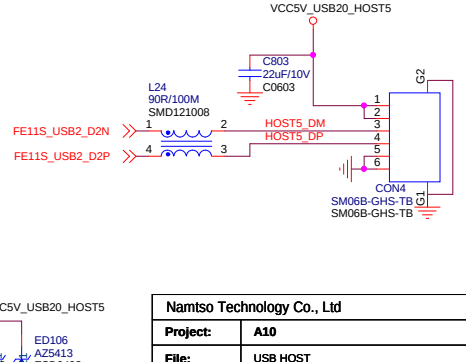
USB20 HOST4





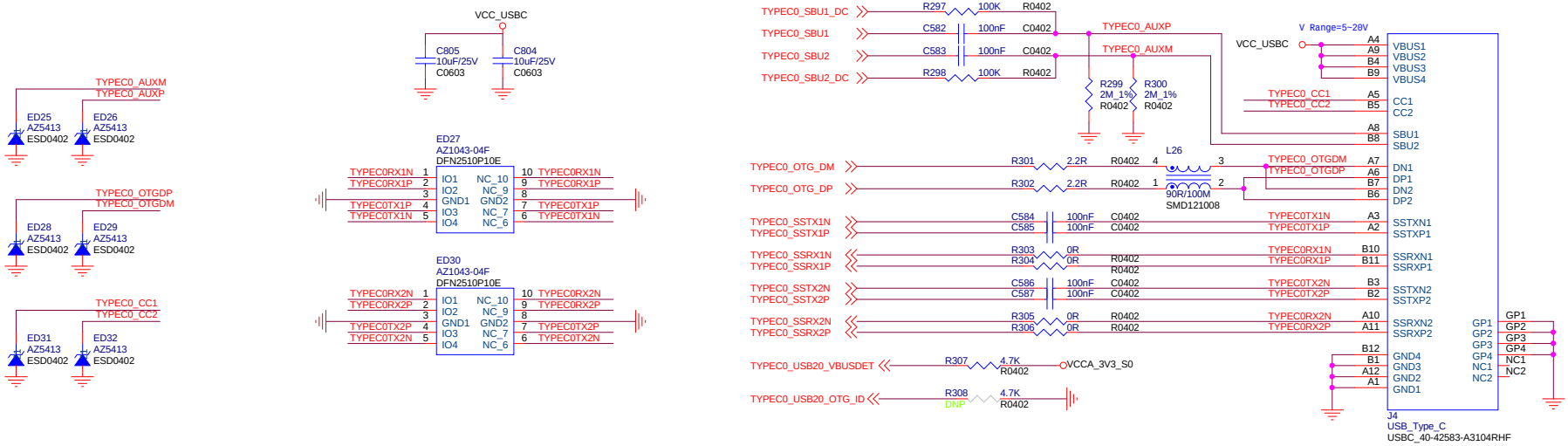
USB20 HOST5



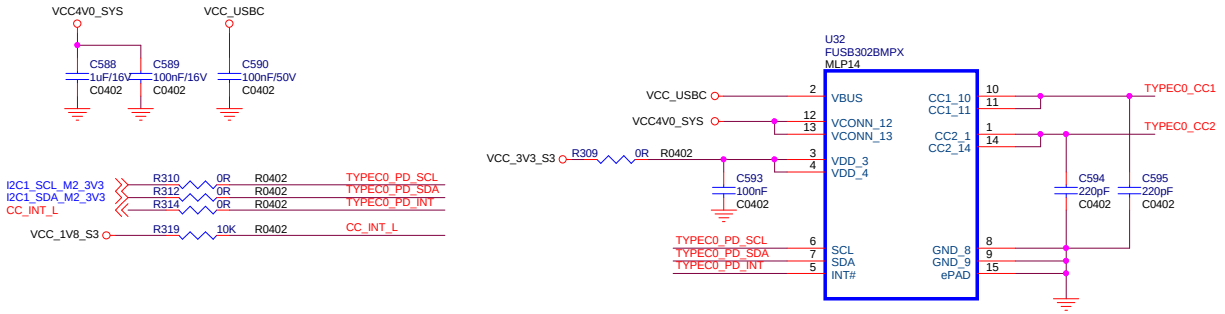


Namtso Technology Co., Ltd			
Project:	A10		
File:	USB HOST		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	25

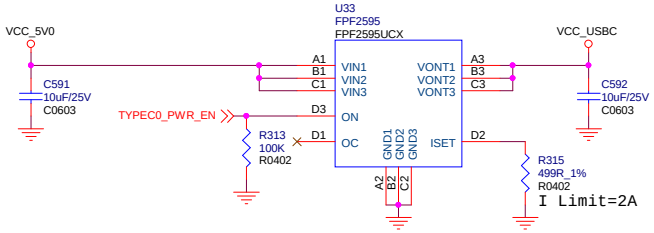
Type-C PORT



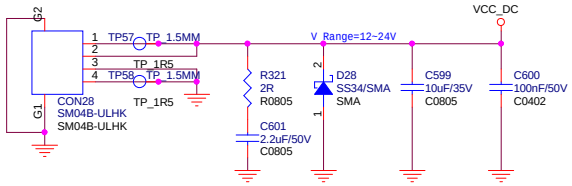
USBC PD



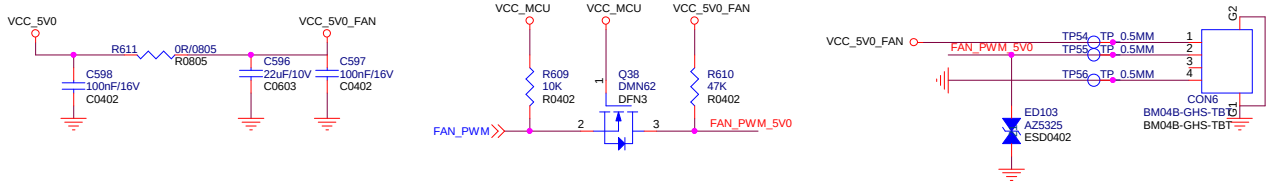
USBC POWER



DC IN

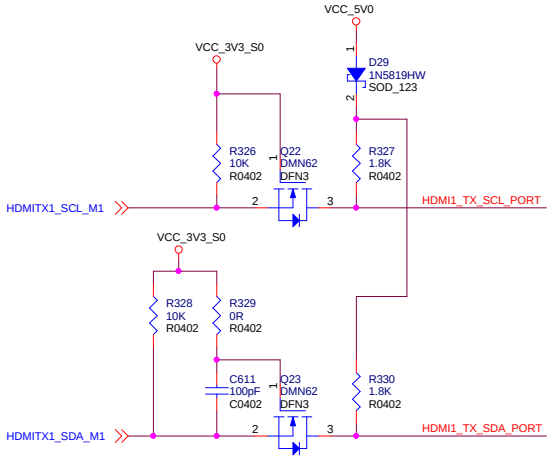


FAN

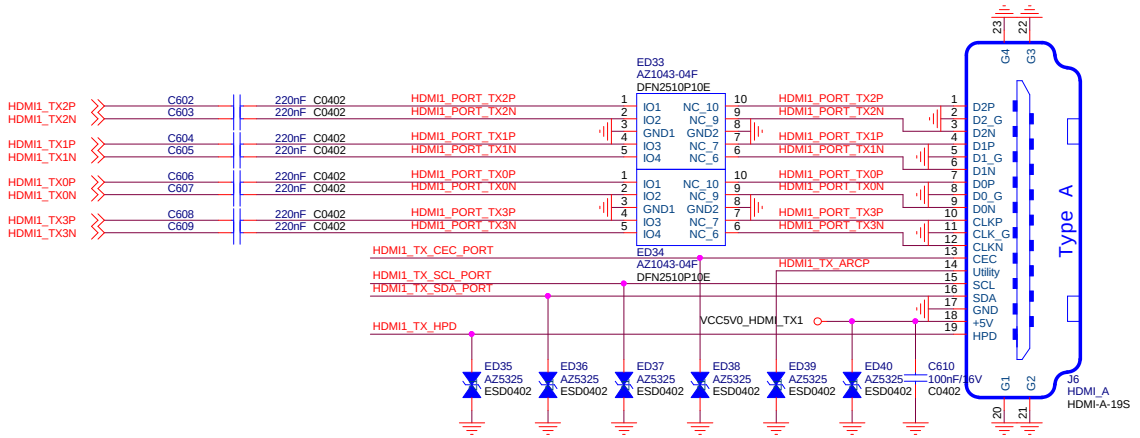


Namtso Technology Co., Ltd			
Project:	**A10**		
File:	**Type-C/DC/FAN**		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	26

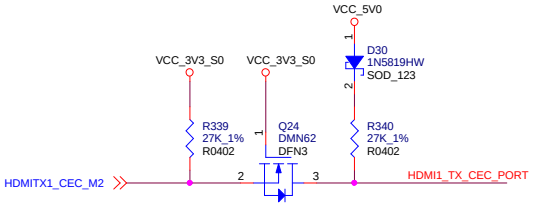
HDMI TX DDC



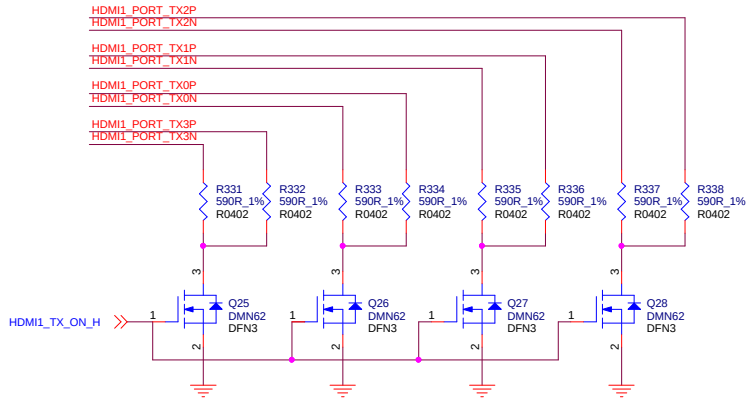
HDMI Jack



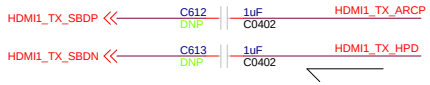
HDMI TX CEC



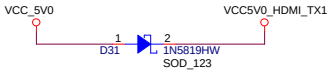
HDMI 2.0/2.1 Switch



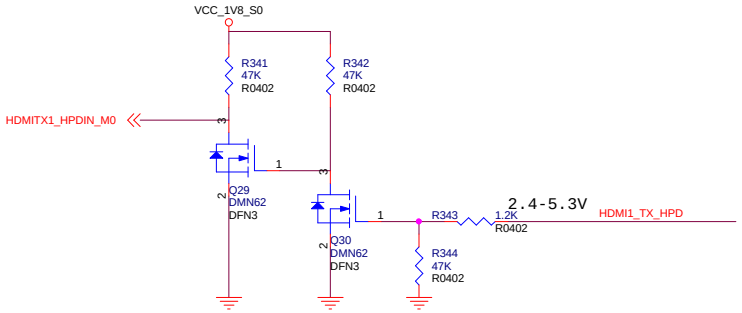
HDMI TX ARC



HDMI Power

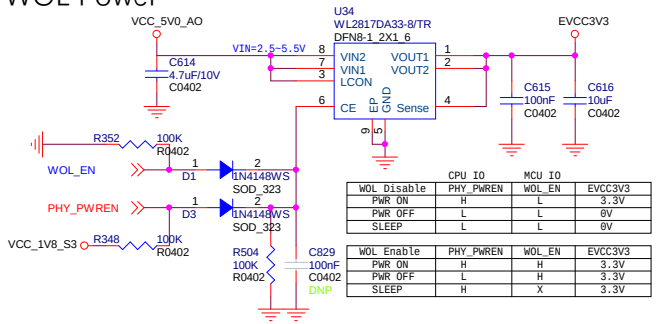


HDMI HPD



Namtso Technology Co., Ltd			
Project:	**A10**		
File:	**HDMI0 TX**		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	27

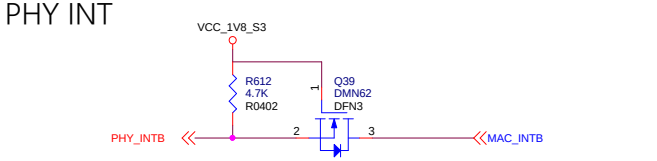
WOL Power



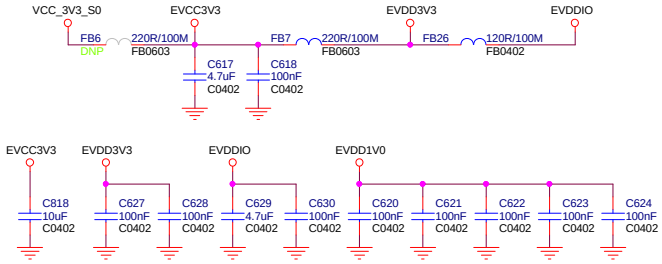
CPU IO		MCU IO	
WOL Disable	PHY_PWREN	WOL_EN	EVCC3V3
PWR ON	H	L	3.3V
PWR OFF	L	L	0V
SLEEP	L	L	0V

WOL Enable	PHY_PWREN	WOL_EN	EVCC3V3
PWR ON	H	H	3.3V
PWR OFF	L	L	3.3V
SLEEP	H	X	3.3V

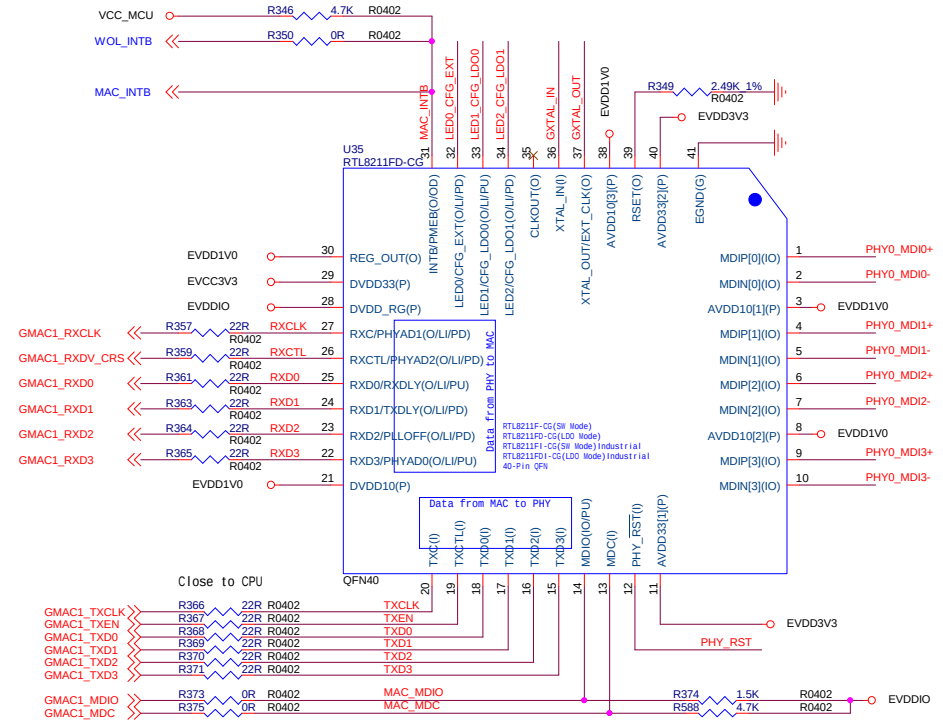
PHY INT



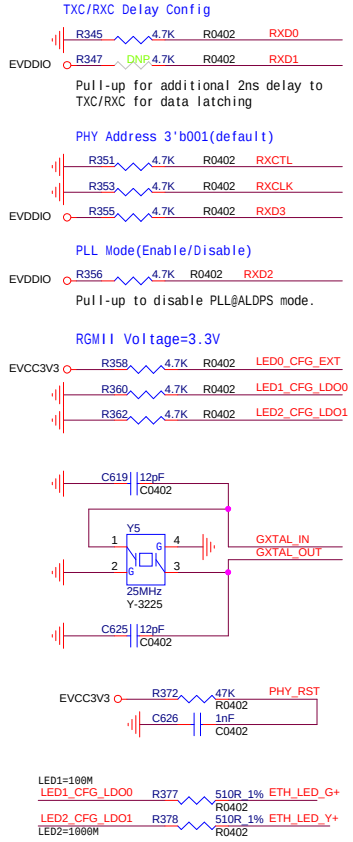
Filter



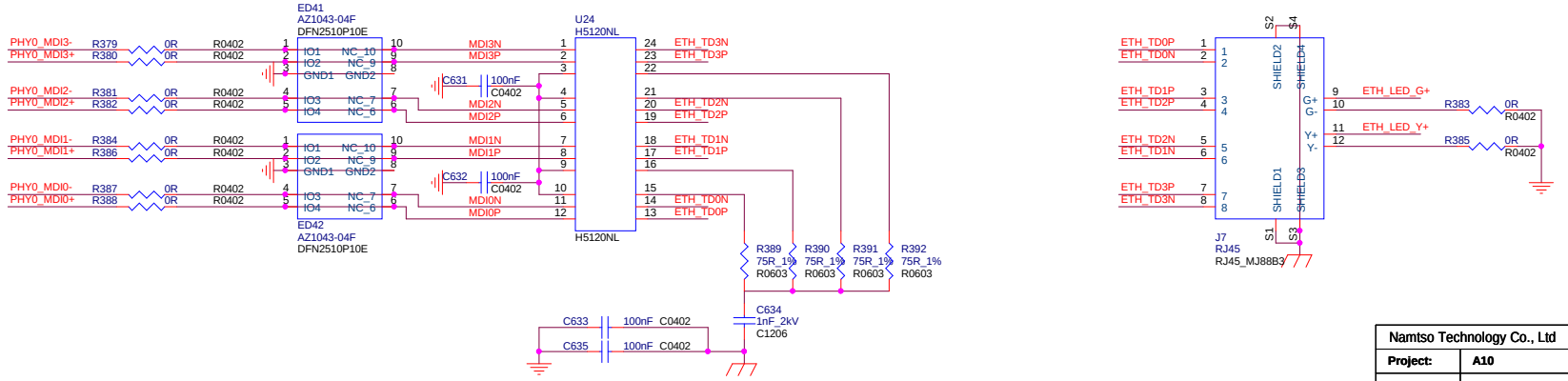
PHY



PHY Config

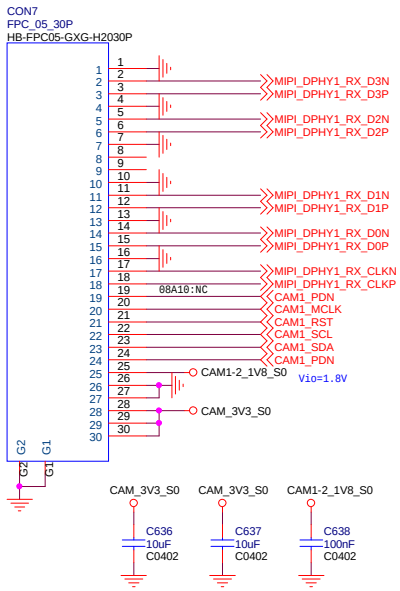


LAN & RJ45

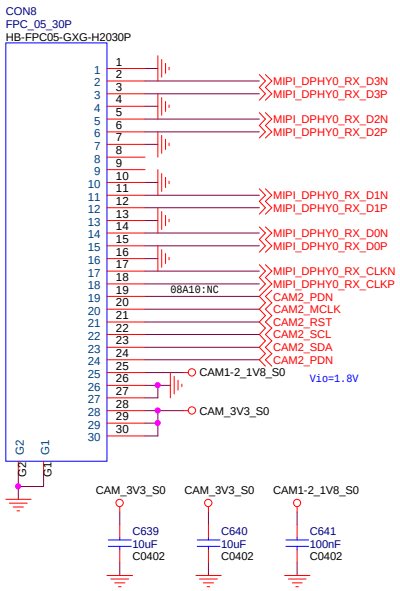


Namtso Technology Co., Ltd			
Project:	A10		
File:	PHT_RGMII		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	28

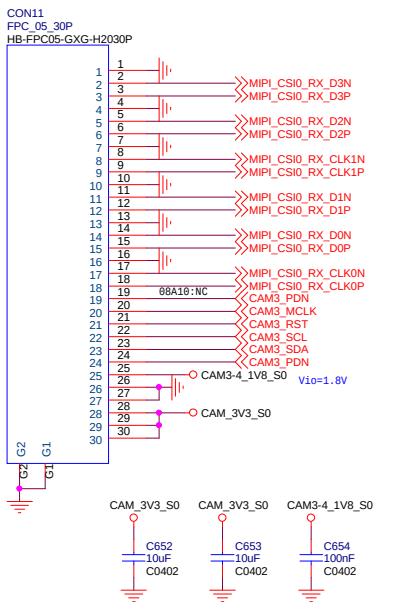
Camera1



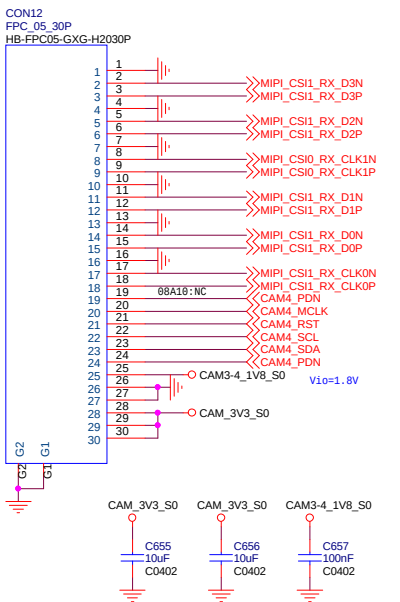
Camera2



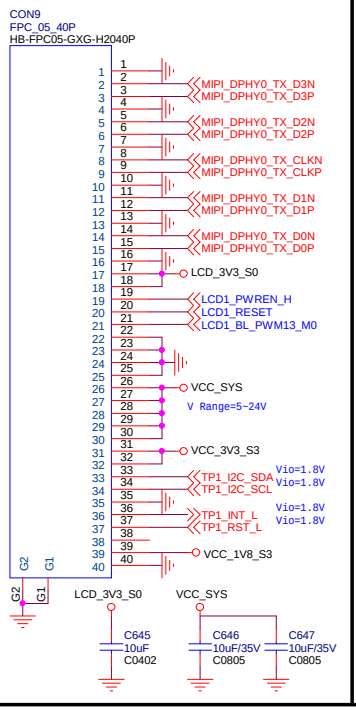
Camera3



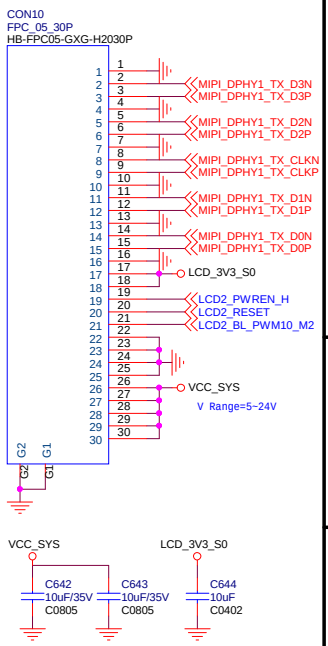
Camera4



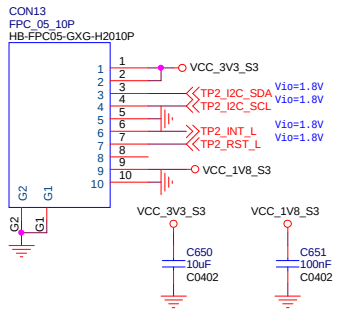
DSI 1



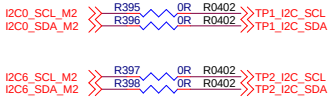
DSI2



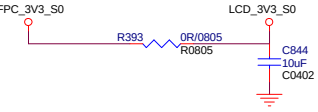
TP



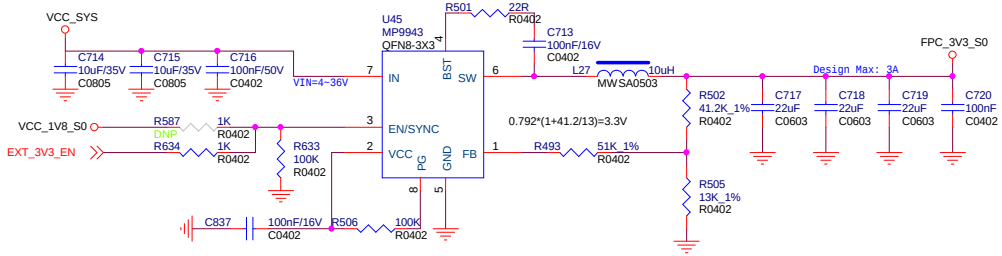
TP I2C



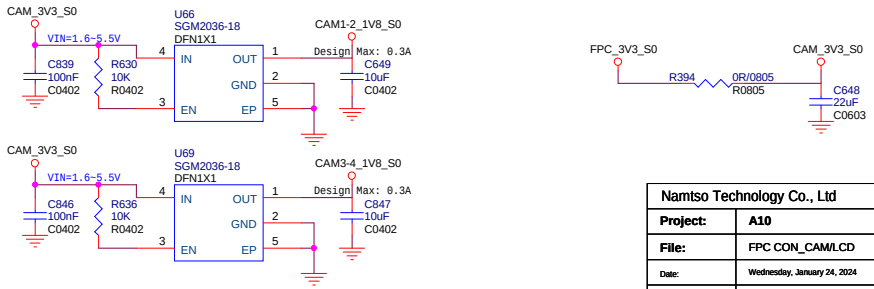
DSI 3V3 PWR



FPC COM PWR

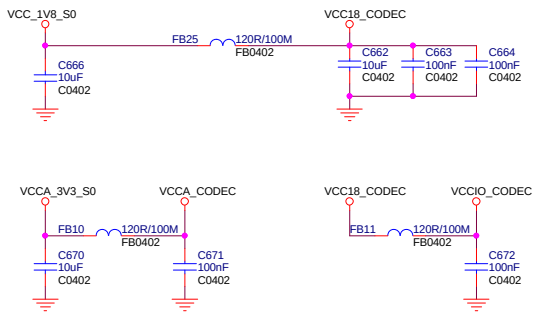


CAM PWR

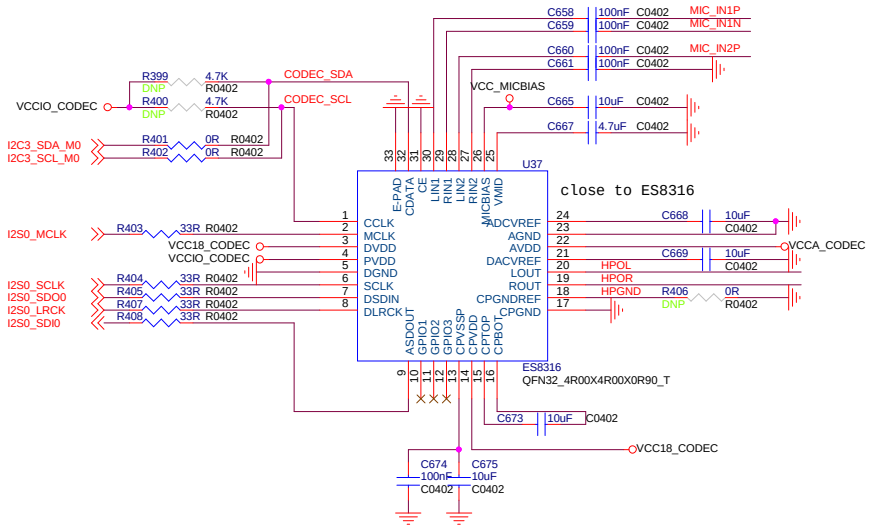


Namtso Technology Co., Ltd			
Project:	**A10**		
File:	**FPC CON_CAM/LCD**		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	29

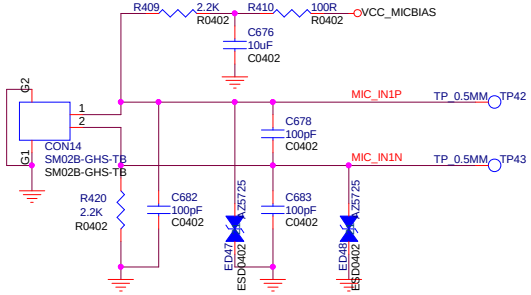
Codec Power



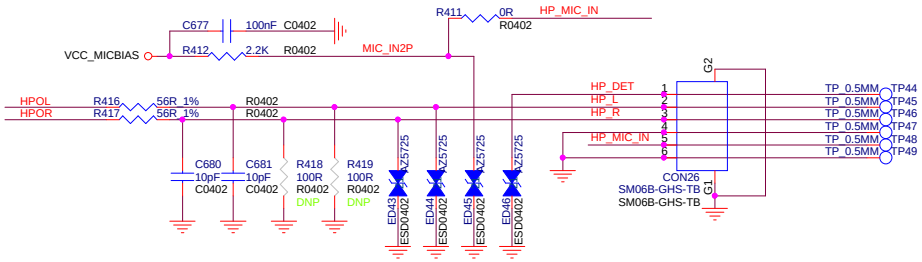
Codec



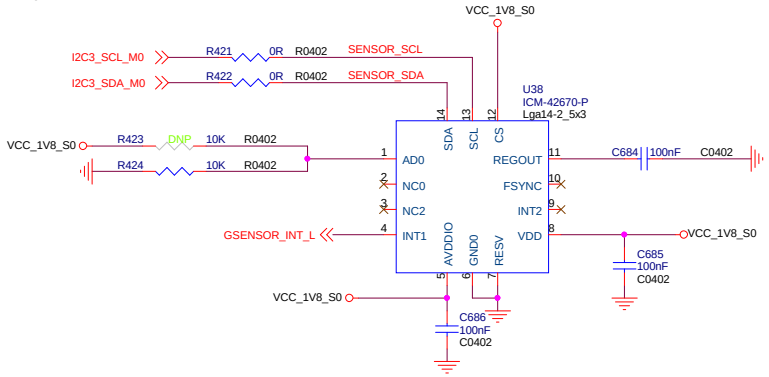
AMIC



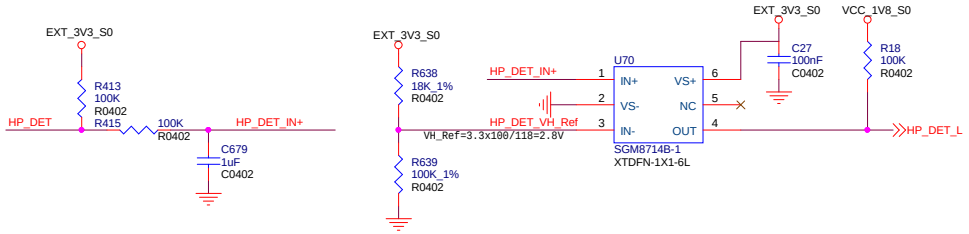
Headphone



Gyroscope+G-sensor

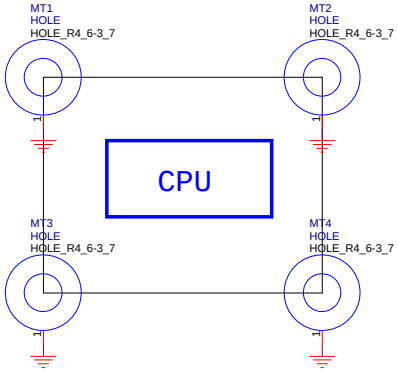


Headphone Detect

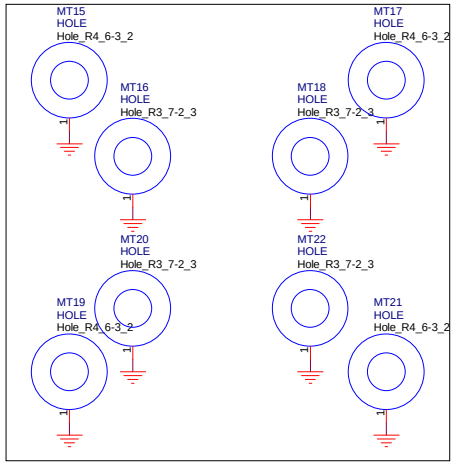


Namtso Technology Co., Ltd			
Project:	**A10**		
File:	**Audio Codec/Gsensor**		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	30

CPU Screw Hole

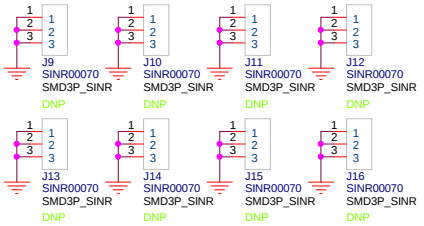


Board Screw Hole

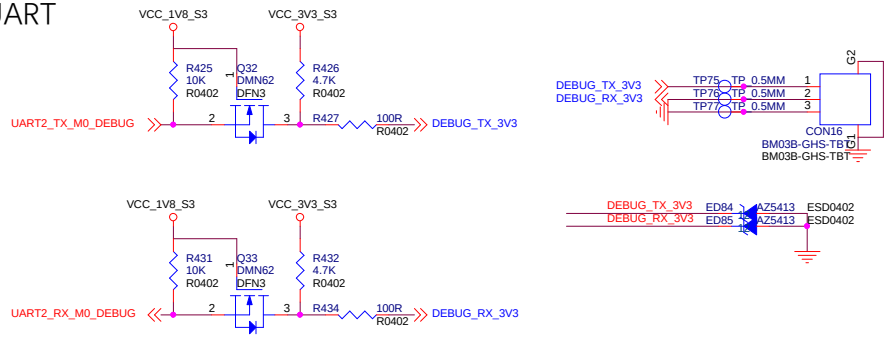


NLink Screw Hole

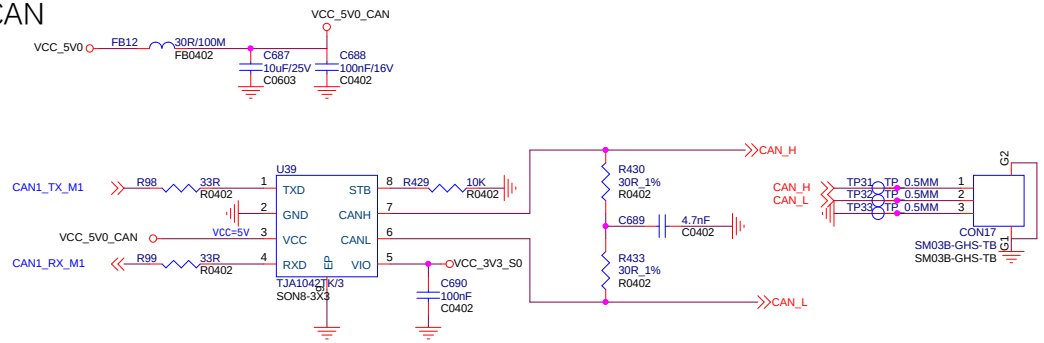
Shield clamp



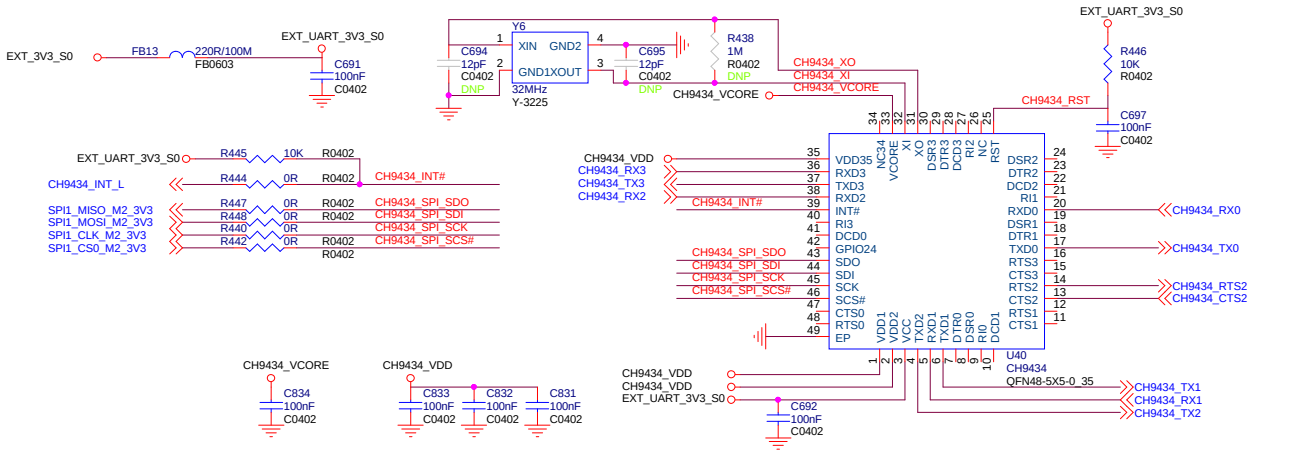
UART



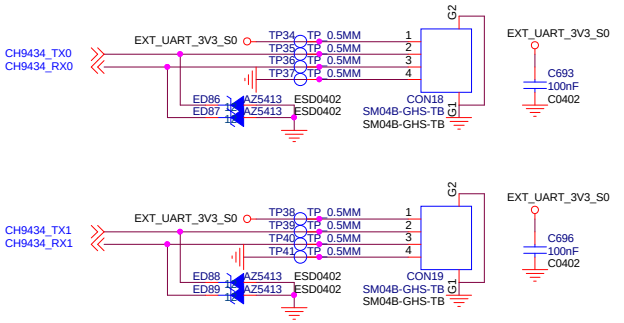
CAN



UART HUB

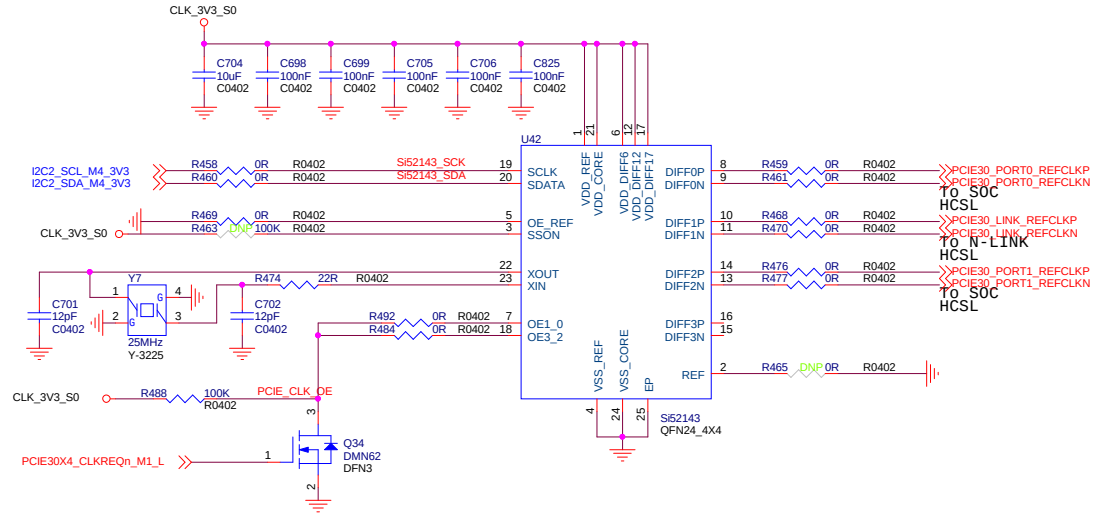


EXT UART CON

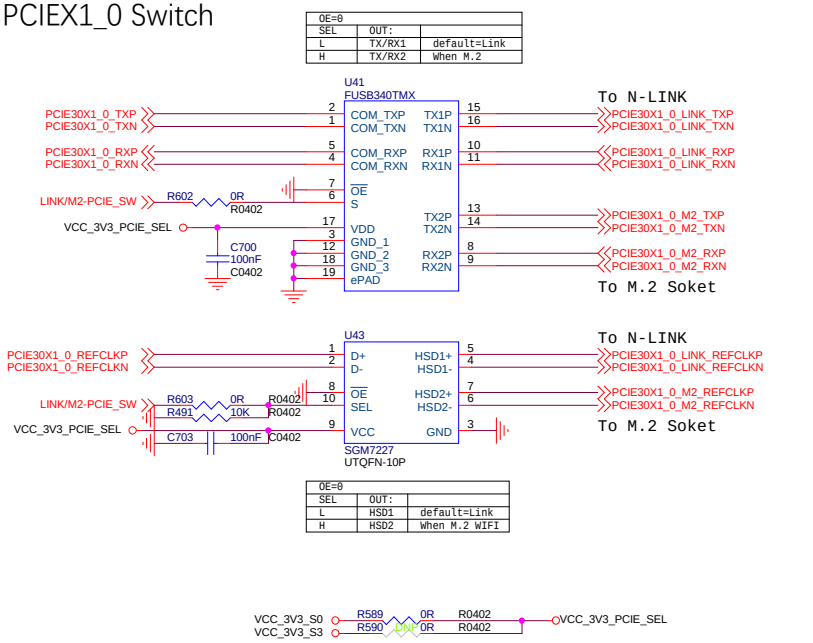


Namtso Technology Co., Ltd			
Project:	A10		
File:	UART/CAN/MISC		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	31

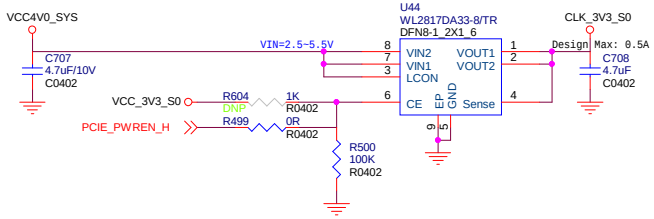
PCIE CLK OUT



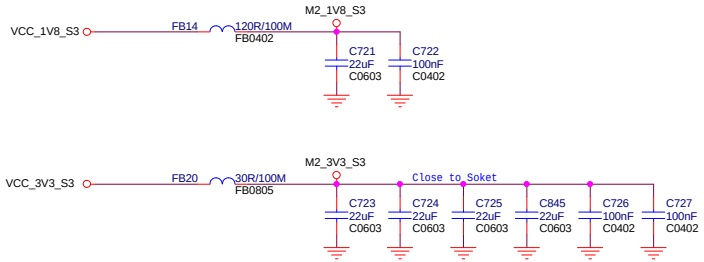
PCIEX1_0 Switch



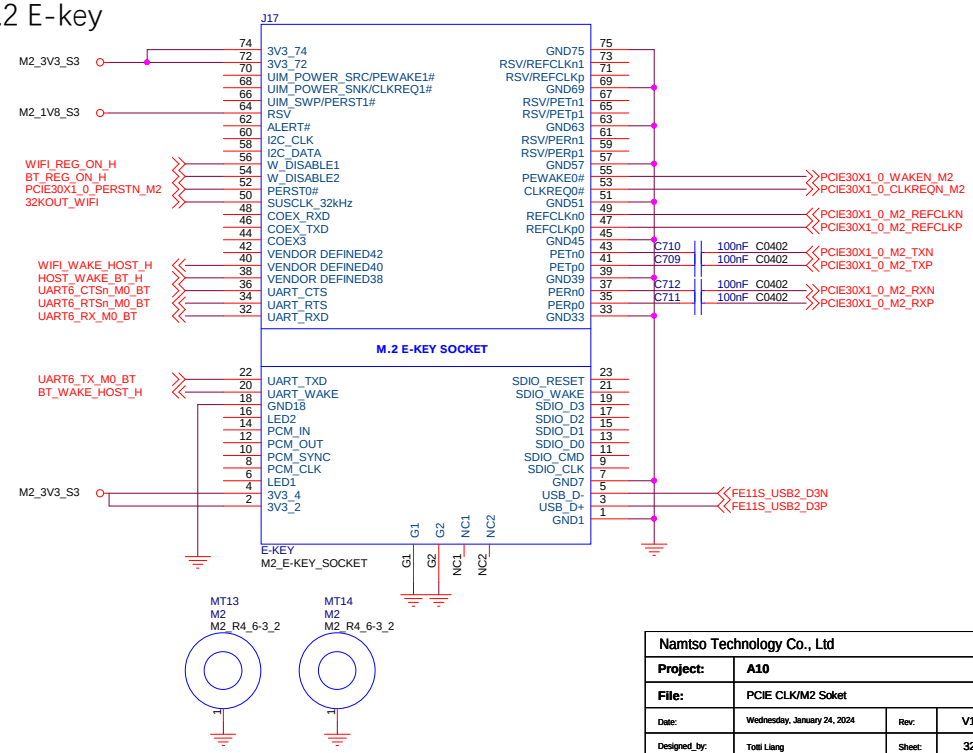
PCIE CLK Power



M.2 Soket Power



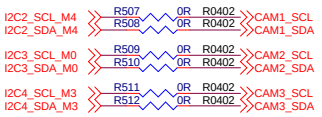
M.2 E-key



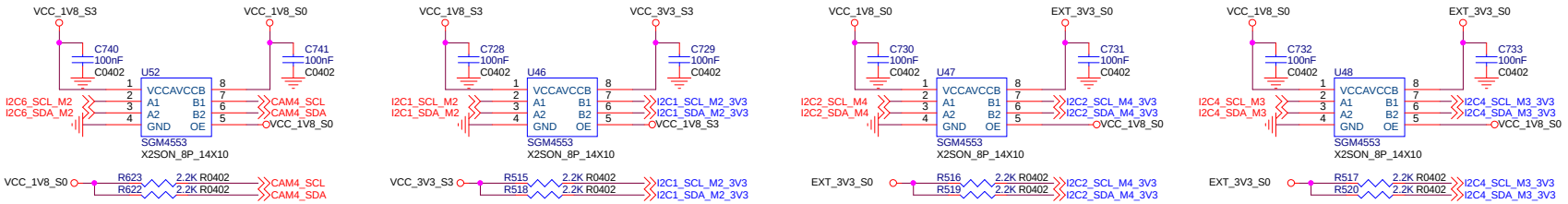
Namtso Technology Co., Ltd			
Project:	A10		
File:	PCIE CLK/M2 Soket		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	32

I2C MAP

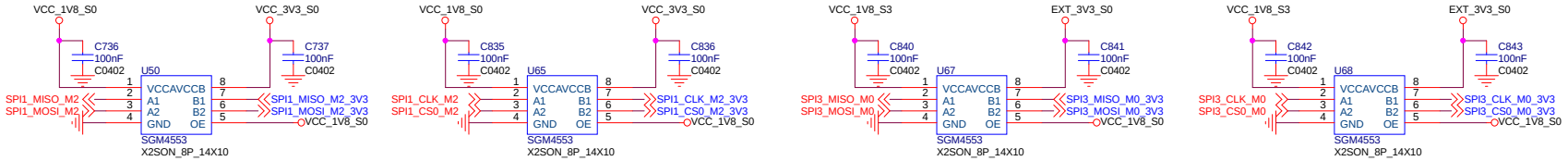
```
I2C0:
1.8V_S3:RK860-2=CPU_BIG0
1.8V_S3:RK860-3=CPU_BIG1/TP1
I2C1:
1.8V_S3:RK860-2=CPU_NPU
3.3V_S3:MCU/RTC/PD IC
I2C2:
1.8V_S0:CAM1
3.3V_S0:EXT2/Si52143
I2C3:
1.8V_S0:CAM2/Gsensor/Codec
I2C4:
1.8V_S0:CAM3
3.3V_S0:LINK_PCIE/EXT1
I2C6:
1.8V_S3:TP2
1.8V_S0:CAM4

I2C5/I2C7/I2C8=NO USE
```



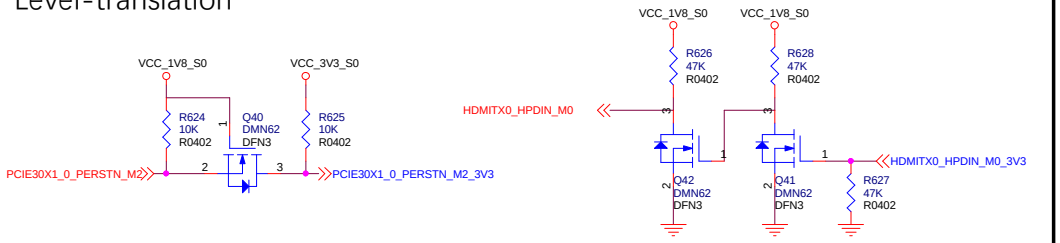
I2C Level-translation



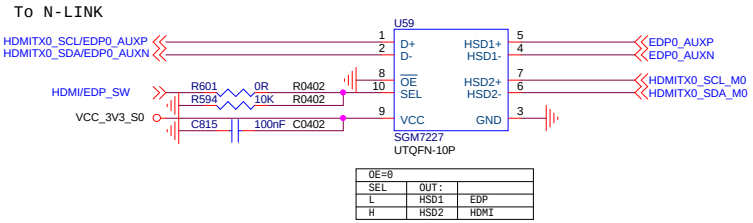
SPI Level-translation



Level-translation

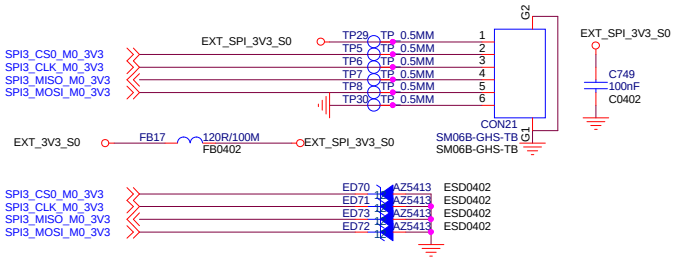


LINK HDMI/EDP SW

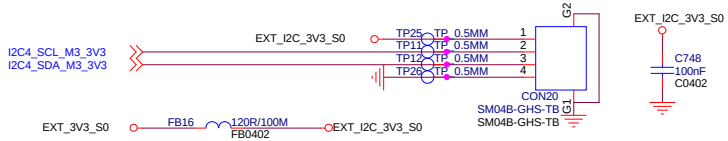


OE=0		
SEL	OUT:	
L	HSD1	EDP
H	HSD2	HDMI

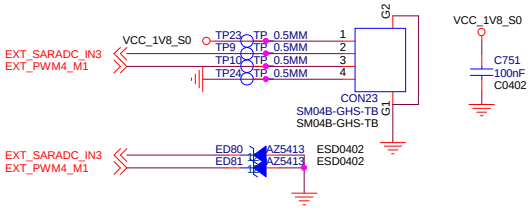
EXT_SPI



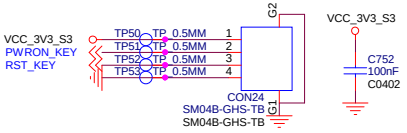
EXT_I2C1



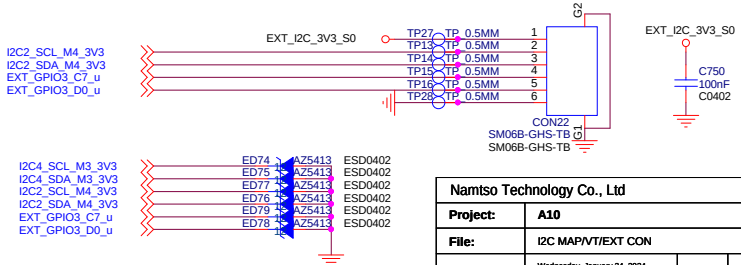
EXT_PWM/ADC



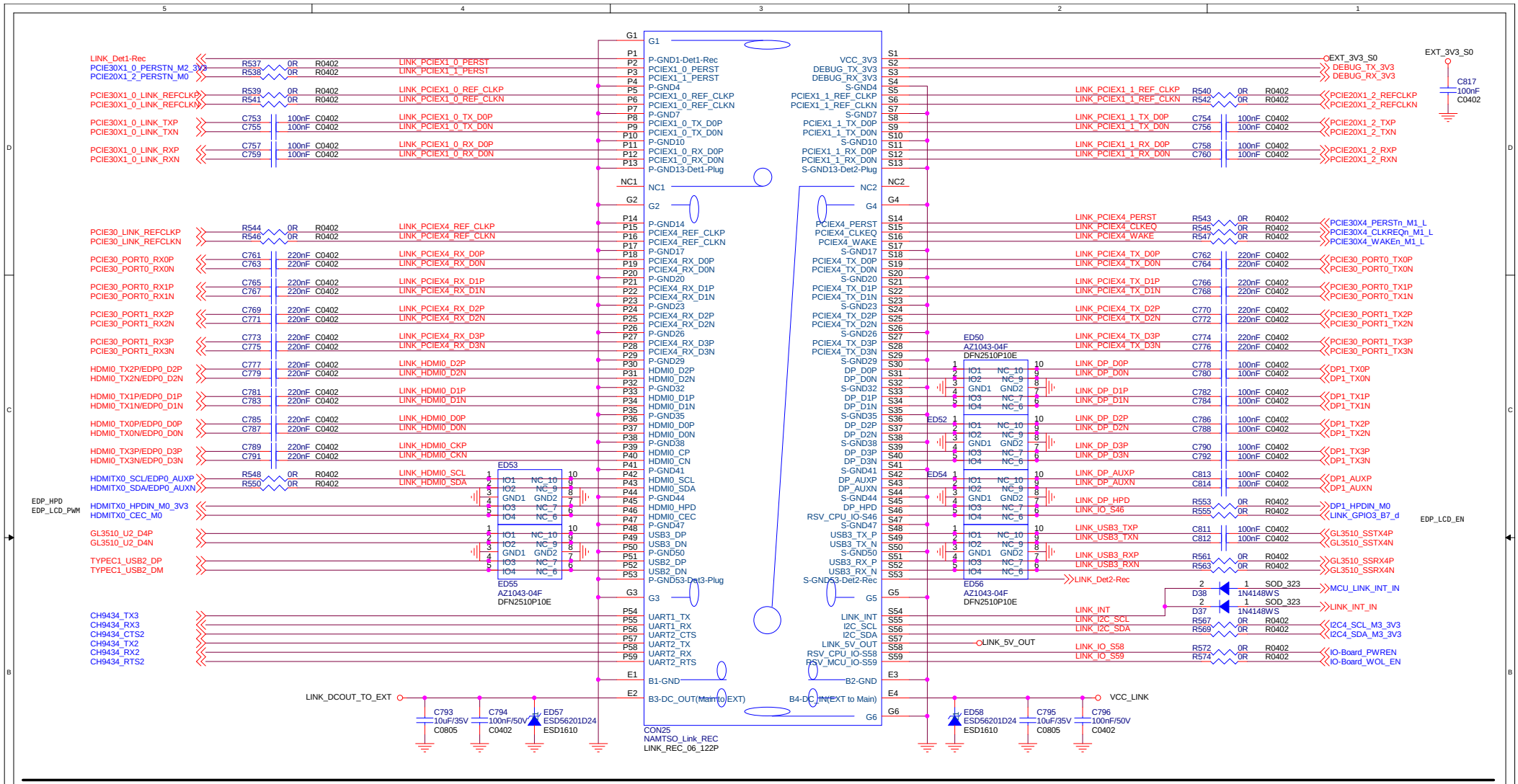
EXT_Buttons



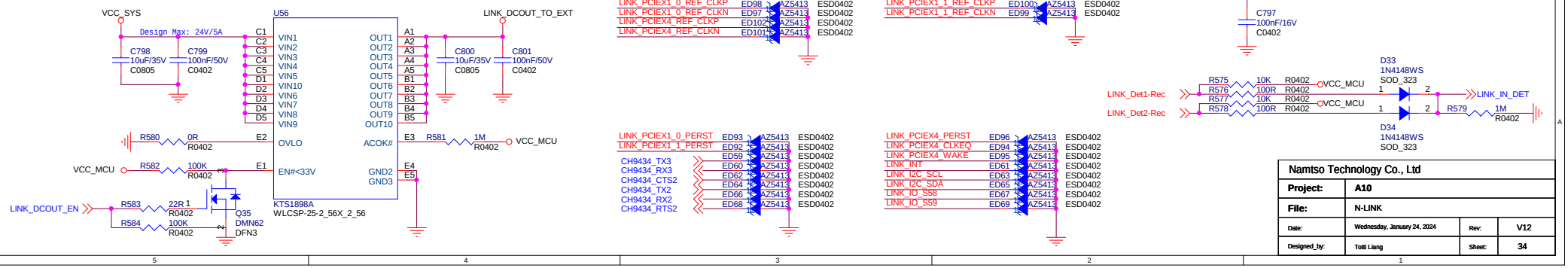
EXT_I2C2



Namtso Technology Co., Ltd			
Project:	A10		
File:	I2C MAP/VT/EXT CON		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	33



LINK_DCOUT_TO_EXT



Namtso Technology Co., Ltd			
Project:	A10		
File:	N-LINK		
Date:	Wednesday, January 24, 2024	Rev:	V12
Designed_by:	Totti Liang	Sheet:	34